DRM DRAWING FORM		
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APPLICATION

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7472500	STGT

REVISIONS

FOR DRAWING REVISION STATUS SEE UNITIZED DOCUMENT AUDIT REPORT (UDAR)

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INTERSTATE ELECTRONICS CORPORATION
A Figgie International Company
1001 E. Ball Road, P.O. Box 3117, Anaheim, California 92803

TITLE
PERFORMANCE SPECIFICATION,
SECOND TDRSS GROUND TERMINAL
(STGT) TEST MODEM

SIZE	CAGE NO.	DRAWING NO.	REV.
A	07421	7472506	C
SCALE	REV IN – FILE DATE 94-4-13	SHEET 1 OF 152	

FORM IEC-038

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APPENDIXES

1.0 SCOPE

1.1 General

This specification defines the performance, design, development, interface, and test requirements for the Test Modem (TM), Interstate Electronics Corporation (IEC) Part Number 7472500, herein also referred to as the unit.

1.2 Purpose

The unit will be used in the Second TDRSS Ground Terminal (STGT) User Service Subsystem (USS) to support the Performance Measuring and Monitoring System (PMMS) Test Equipment (PTE). The PTE is used to verify forward and return USS TDRSS links and equipment. The Tracking and Data Relay Satellite System (TDRSS) is a major segment of NASA's Space Network.

2.0 APPLICABLE DOCUMENTS

The following documents of the exact date of issue, unless otherwise noted, form a part of this specification to the extent specified herein. The order of precedence of this specification relative to the referenced documents shall be as established in 3.8.

2.1 Government Documents

2.1.1 Specifications

2.1.1.1 Federal

None.

2.1.1.2 Military

MIL-C-5541	Chemical Conversion Coatings on Aluminum and Aluminum Alloys, Revision D, 28 February 1989
MIL-C-39019	Magnetic Low-Power, Sealed, Trip-Free, Circuit Breakers, General Specifications for Supplement 1, July 1974
MIL-P-53030	Primer Coating, Epoxy, Water Reducible, Lead Chromate Free December 1983
MIL-P-55110	Printed Wiring Boards, General Specification for Revision D, December 1984
MIL-S-5002	Surface Treatments and Inorganic Coatings for Metal Surfaces of Weapons Systems, Revision D, 30 November 1989

2.1.1.3 National Aeronautics and Space Administration (NASA) - None.

2.1.2 Standards

2.1.2.1 Federal

FED-STD-595	Federal Standard Colors - Paint Revision A, through Notice 9 May 1985

2.1.2.2 Military

MIL-STD-130	Identification Marking of U.S. Military Property Revision G, 11 Oct 88
MIL-STD-454	General Requirements for Electronic Equipment Revision K, Notice 3, 26 February 1987

MIL-STD-461	Electronic Emission and Susceptibility Requirements for the Control of Electromagnetic Interference, Part 3 Revision C, August 1986
MIL-STD-462	Electromagnetic Interference Characteristics, Measurement of. Through Notice 1, February 1971
MIL-STD-975	NASA Standard Electrical, Electronic, & Electromechanical (EEE) Parts List Revision H, 30 June 1989
MIL-STD-1130	Connections, Electrical, Solderless, Wrapped Revision B, December 1978
MIL-STD-1472	Human Engineering Design Criteria for Military Systems, Equipment and Facilities Revision D, 14 March 1989
MIL-STD-1553B	Digital Time Division Command/Response Multiplex Data Bus. Notice 2, 08 September 1986

2.1.2.3 NASA

STDN No. 101.2	Space Networks Users' Guide. GSFC. Revision 6, September 1988.
STDN No. 108	PN Codes for Use with the Tracking and Data Relay Satellite System (TDRSS). December 1976
STDN No. 270.7	GSFC Grounding System Requirements July 1989
STDN No. 927.1	STGT Configuration Management Plan March 1987
STDN No. 927.2	STGT Performance Verification Plan May 1987
STDN No. 927.4	STGT Quality Assurance Plan May 1987

2.1.3 Drawings

None.

2.1.4 Other Publications

IRIG-STD 104-70	IRIG Standard Serial Binary Code Formats August 1970

MIL-HDBK-217	Reliability Prediction of Electronic Equipment Notice 1, 2 January 1990
NHB 6000.1C	Requirements for Packaging, Handling, and Transportation June 76
FCC R&R	FCC Rules and Regulations, Part 15 Subpart J for Microprocessor Controlled Devices No date given.

2.2 Non-Government Documents

2.2.1 Specifications

2.2.1.1 General Electric Corporation/Aerospace

GES-STGT-1323	SSA Equipment HWCI Specification (HWCI No. 5). (aka STGT-HE-04-5) Revision 2, September 1990
GES-STGT-1325	KSA Low Data Rate Equipment HWCI Specification (HWCI No. 7). (aka STGT-HE-04-07) Revision 2, September 1990
GES-STGT-1328	Multiple Access Receiver/Transmitter HWCI Specification (HWCI No. 10). (aka STGT-HE-04-10) Revision 2, September 1990
STGT-HE-06-2	GE Hardware/Hardware Interface Control Document for STGT Appendix H Interface Control Document for the Performance Measurement Test Equipment (PTE) and the USS Subsystem Controller (SSC)/USS ADPE December 1990 through DCN 002

2.2.1.2 Interstate Electronics Corporation - None.

2.2.2 Standards
None.

2.2.3 Drawings

2.2.3.1 Interstate Electronics Corporation

7472502	Drawing Tree Test Modem Assembly. 23 October 1989
C901E3860	STGT Unit Test Matrices

2.2.4 Other Publications

NFPA 70	National Electric Code (NEC), 1987

2.2.4.1 General Electric Corporation

SOW-GE-STGT-8701	Statement of Work (SOW) for USS Equipment SSA Equipment HWCI KSAR Low Data Rate Equipment HWCI MA RCVR/XMTR Equipment HWCI. Latest Revision of November 1989

2.2.4.2 Interstate Electronics Corporation

C901E3331	Configuration Management Plan and Procedures for Second TDRSS Ground Terminal. Contract No. F14000-U-16507 SDRL Items CM-01 and CM-02. December 1989
C901-812	Supporting Engineering Analysis Data for Second TDRSS Ground Terminal. Contract No. F14000-U-16507 SDRL Item HE-08. April 1990
C903F3379	Training and Training Equipment Plan Contract No. F14000-U-16507 SDRL LO-02 October 1990
	Maintenance Manual, Level 1 for Test Modem Contract No. F14000-U-16507 SDRL OP-06 December 1990 PRELIMINARY

2.2.4.3 Test Equipment Manuals

2.2.4.3.1 Aydyn Computer and Monitor

298-0798	Operation and Maintenance Manual Data Transmission Test Set (DTTS) Model 604MI P/N 356-00210506 August 1989

2.2.4.3.2 Hewlett Packard

Manual Part No. 03708-90001	Operation Manual 3708A Noise and Interference Test Set August 1984
Manual Part No. 05316-900014	Operating and Service Manual 5316B 100 MHz Universal Counter September 1987

13.0 REQUIREMENTS

3.1 Prime Item Definition

The Test Modem is an integral part of the Performance Measuring and Monitoring System (PMMS) Test Equipment. The PMMS Test Equipment (PTE) consists of a Test Modem (TM) provided by Interstate Electronics Corporation and commercial test equipment provided by General Electric (GE). Separate sets of PMMS Test Equipment are contained in each K-Band Single Access (KSA) Low Data Rate Equipment, S-Band Single Access (SSA) Equipment, and Multiple Access (MA) Receiver/ Transmitter hardware configuration item (HWCI) used in the STGT User Service Subsystem (USS). This specification provides requirements for the Test Modem.

a. Allocation of Functions

For the purposes of requirements allocation, the TM will be considered to consist of two functional entities; the Forward Demodulator and the Return Modulator. The Forward Demodulator is used in the PTE with one of the GE furnished bit error rate test sets (BERTS), called the Forward Command Channel BERTS. The Return Modulator is used in the PTE with the following GE furnished equipment; two BERTS (called the Return I and Q Channel BERTS), one Eb/No test set, and two time interval counters (TIC).

b. Forward Demodulator Functions

The TM shall provide the following essential Forward Demodulator functions, as required:

(1) Provide test data and clock for use by the Modulator/Doppler Predictor (MDP). The data and clock will be routed to the MDP through the Primary Interface.

(a) Local data - Provide local data and clock by commanding and controlling the Forward Command Channel BERTS.

(b) External data - External forward Command Channel data from the Data Interface System (DIS) may be used with the PTE.

(2) Receive a modulated forward service IF from the Primary Interface.

(3) Provide Doppler correction in the Forward Demodulator, including the capability to:

(a) Receive Doppler updates (ephemeris data) from the 1553B data bus;

(b) Maintain a Forward Model of Doppler compensation and control performed on the forward link.

(4) Despread and track the received PN spread signal (one channel only).

(5) Provide PN code epoch and clock for range measurement.

(6) Demodulate and track the carrier.

(7) Recover carrier for Doppler measurement.

(8) Support coherent turnaround of the recovered carrier for use by the Return Modulator.

(9) Recover symbol clock and detect symbols.

(10) Provide convolutional decoding for recovered symbols.

(11) Provide format conversion of recovered data so that the output data stream is NRZ-L.

(12) Provide as outputs from the TM to the Primary Interface the recovered forward Command Channel data with synchronous clock.

(13) For internally generated data (Local Data), route the recovered Forward Command Channel data and clock to the Forward Command Channel BERTS.

(14) Provide control of the Forward Command Channel BERTS and measure the Forward Command Channel bit error rate (BER).

(15) Provide an estimate the Forward Command Channel Eb/No.

c. <u>Return Modulator Functions</u>

The TM shall provide the following essential Return Modulator functions, as required:

(1) Provide test data and clocks for use by the Return Modulator.

(a) <u>Local Data</u> - Provide local "RZ-L format data and clock by commanding and controlling the Return I and Q Channel BERTS.

(b) <u>External Data</u> - Receive external NRZ-L data and clock from the Primary Interface and provide appropriate bit synchronization.

(c) <u>Local/External</u> - Test data and clocks may be local and/or external in that the unit may provide local I data and clock while accepting external Q data and clock, and vice versa.

(2) Provide data formatting, convolutional encoding, symbol formatting, and interleaving of Return Channel data.

(3) As commanded, coherently derive a Return Channel IF carrier from the recovered Forward Channel IF carrier, or else independently generate a Return Channel IF carrier.

(4) When generating an independent Return Channel IF carrier, follow a commanded frequency profile using Doppler updates (ephemeris data) from the 1553B data bus.

(5) Generate PN codes and clocks.

(6) PSK modulate the Return Channel IF carrier with Return Channel Data and PN Codes.

(7) Provide the capability to adjust the I to Q channel power ratio.

(8) Provide command and control of the Eb/No Test Set to allow the Return Channel modulated signal to be set to a commanded C/No value.

(9) Provide the modulated signal as an output to the Primary Interface at one of two selectable IF output ports (8.5 MHz or 370 MHz).

(10) Accept recovered Return Channel data and clocks from the Integrated Receiver via the Primary Interface.

(11) Route the recovered Return Channel data and clocks to the Return I and Q Channel BERTS and when the data is internally generated (local data), perform bit error rate (BER) measurements.

(12) For internally generated Return Channel data, provide Data Delay Measurements by commanding and controlling the Time Interval Counters.

(13) The TM shall provide the conditioned basehand data, PN spread if applicable, to the control HWCI. Synchronous clock shall be provided along with data when the data is not PN spread.

(14) The TM shall provide the unmodulated 370 MHz carrier to the control HWCI.

(15) The TM shall provide the resultant 8.5 MHz test IF signal to the control HWCI.

d. Functions Common to Forward and Return

The TM shall provide the following essential functions, which are common requirements for the Forward Demodulator and the Return Modulator:

(1) Generate status data, including self-test and fault isolation information, both to the front panel and the MIL-STD-1553B data bus.

(2) Communicate with the Primary Interface configuration items via a MIL-STD-1553B data bus as described in paragraph 3.1.2.2.2 and appendix II.

(3) Communicate with the GE furnished commercial test equipment via an IEEE-488 data bus.

(4) To support maintenance and operation, provide front panel and maintenance panel controls, indicators, and test points, as specified.

3.1.1 Prime Item Diagrams
The TM will be used to support Forward and Return test loops.

3.1.1.1 Forward Loop Tests - Forward loop tests are used to verify the operational readiness of forward link equipment, including the Modulator/Doppler Predictor. Forward loop tests are illustrated in figure 1 for SSA, in figure 2 for KSA, and in figure 3 for MA. These configurations are quite similar and each includes the following:

a. Short loopback
b. Intermediate loopback
c. End-to-End loopback

3.1.1.2 Return Loop Tests - Return loop tests are used to verify the operational readiness of return link equipment, including the Integrated Receiver. Return loop tests are illustrated in figure 4 for SSA, in figure 5 for KSA, and in figure 6 for MA. These configurations are quite similar and each includes the following:

a. Very short loopback (KSA only)
b. Short loopback
c. Intermediate loopback
d. Long loopback
e. End-to-End loopback

3.1.1.3 Test Modem Interfaces - The functional and physical relationships of the TM with the Primary Interface and with the Test Equipment Interface are diagrammed in figure 7.

3.1.1.4 Unit Diagrams - The unit block diagram is shown in figure 8. The functional flow of the unit is provided in figure 9. The unit front panel is given in figure 10. The maintenance panel is given in figure 11, and the unit back panel is illustrated in figure 12.

3.1.2 Interface Definition
Consistent with the criteria for configuration item identification in STDN No. 927.1, section 2.3.2, the TM will be treated as a single configuration item and may be used interchangeably in the SSA Equipment, KSA Low Data Rate Equipment, or MA Receiver/ Transmitter hardware configuration items (HWCI). The unit has three interfaces; (1) a back panel interface, (2) a front panel interface, and (3) a maintenance panel interface. The back panel interface is divided into a Primary Interface and a Test Equipment Interface.

a. Connectors and Signals - Table I shows the connector termination and signal identification for the back panel interfaces to the Primary Interface. Table II lists signals and connectors associated with the Test Equipment Interface. Table III gives the maintenance panel connectors. Table IV shows additional signals and connectors. Table V provides identification of connector types.

b. Functional and Physical Interfaces - The primary control and interface with the unit is via the back panel interface. Back panel interfaces are further identified as either Primary Interface signals, or as Test Equipment Interface signals. Note that the unit's interfaces all begin and end at the unit. That is no cables or power cords are provided with the unit.

c. Primary Interface - On one side of the Primary Interface is the Test Modem provided by Interstate Electronics Corporation. On the other side are all other configuration items, excluding the Test Equipment, which are controlled by General Electric.

d. Test Equipment Interface - On one side of the Test Equipment Interface is the TM. On the other side are the units which make up the GE furnished test equipment, herein also called the Test Equipment:

(1) Forward Command Channel BERTS, Aydin 604MI-STGT
(2) Return I Channel BERTS, Aydin 604MI-STGT
(3) Return Q Channel BERTS, Aydin 604MI-STGT
(4) Eb/No Test Set, Hewlett-Packard 3708A
(5) I Channel Time Interval Counter, Hewlett-Packard 5316B
(6) Q Channel Time Interval Counter, Hewlett-Packard 5316B
(7) IEEE-488 Data Bus

For the purposes of this specification, these units may be treated as a single configuration item whose interface to the TM is the Test Equipment Interface.

e. Jitter Test Interface - Back panel connectors J113 and J114 are provided on the unit back panel to support contractor defined jitter tests.

3.1.2.1 Allocation of Interfaces - As with the allocation of functional requirements, interfaces are defined for the Forward Demodulator and the Return Modulator. Other interfaces are common to both the forward and return parts of the TM. Interfaces with the TM are; (1) the Primary Interface, (2) the Test Equipment Interface (treated as a single configuration item) and, (3) the operator via the front panel or maintenance panel.

3.1.2.1.1 Common Interfaces - The unit shall provide the following interfaces for signals which are common to both forward and return parts of the TM:

a. Primary Interface;

(1) Primary AC Power
(2) MIL-STD-1553B Data Bus
(3) Common Time and Frequency System

b. Test Equipment Interface:

(1) IEEE-488 Data Bus

3.1.2.1.2 Forward Demodulator Interfaces - The unit shall provide the following interfaces for the Forward Demodulator functions in the TM:

a. Primary Interface:

(1) PTE Baseband Command Data and Clock Outputs
(2) PTE 370 MHz IF Input
(3) Recovered Forward Data and Clock Outputs

b. Test Equipment Interface:

(1) Command Channel Transmit Clock Output
(2) Command Channel Data Input
(3) Command Channel Received Data and Clock Outputs

3.1.2.1.3 Return Modulator Interfaces - The unit shall provide the following interfaces for the Return Modulator Functions in TM:

a. Primary Interface

(1) PTE 370 MHz IF Output
(2) PTE 8.5 MHz IF Output
(3) PTE Low Data Rate Baseband Output Data and Clock
(4) PTE Baseband I and Q Data and Clock Inputs
(5) I and Q Simulated User Return Data and Clock Inputs

b. Test Equipment Interface:

(1) 70 MHz IF (all signal) Output
(2) 70 MHz IF (signal plus noise) Input
(3) I Channel Transmit Clock Output
(4) I Channel Data Input
(5) I Channel Received Data and Clock Outputs
(6) Q Channel Transmit Clock Output
(7) Q Channel Data Input
(8) Q Channel Received Data and Clock Outputs

3.1.2.2 Primary Interface Signals

3.1.2.2.1 Primary AC Power - Power will be provided to the unit from the Primary Interface. The unit shall be designed to utilize Primary AC Power which possesses the signal characteristics and unit interface requirements described in table VI.

3.1.2.2.2 MIL-STD-1553B Data Bus - The unit shall communicate, on either of two 1553 buses, with the Primary Interface via a MIL-STD-1553B Digital Time Division Command/Response Multiplex Data Bus, herein also called the data bus. The unit shall be configured as a remote terminal on the data bus. The associated Primary Interface will provide the bus controller. The unit shall meet the interface requirements of STGT-HE-06-2, Appendix H. A list of messages and a description of data bus characteristics are given below:

a. Data Bus Commands - Messages from the bus controller to the TM remote terminal are called commands. The commands may be allocated to General Functions, Forward Demodulator Functions, and Return Modulator Functions.

(1) General Function Commands:

(a) PTE_SET_STATE_COMMAND
(b) PTE_GENERAL_CONFIGURATION_COMMAND
(c) PTE_DOWNLOAD_COMMAND
(d) PTE_EPHEMERIS_DATA_COMMAND

(2) Forward Demodulator Commands:

(a) PTE_DEMOD_SPECIFIC_CONFIGURATION_COMMAND
(b) PTE_DEMOD_COMMON_CONFIGURATION_COMMAND
(c) PTE_DEMOD_START_ACQUISITION_COMMAND
(d) PTE_DEMOD_START_PN_MODEL_COMMAND
(e) PTE_DEMOD_START_FWD_BER_TEST_COMMAND
(f) PTE_DEMOD_RANGE_CHANNEL_REACQUISITION_COMMAND

(3) Return Modulator Commands:

(a) PTE_MOD_CONFIGURATION_COMMAND
(b) PTE_MOD_START_SERVICE_COMMAND
(c) PTE_MOD_START_RTN_BER_TEST_COMMAND
(d) PTE_MOD_MEASURE_TIME_INTERVAL_COMMAND

b. Data Bus Reports - Messages from the TM remote terminal to the bus controller are called status reports. They may be listed as general reports, Forward Demodulator reports, or Return Modulator reports.

(1) General Reports:

(a) PTE_GENERAL_STATUS_REPORT
(b) PTE_EXTENDED_BIT_REPORT
(c) PTE_BER/TIC_MEASUREMENTS_REPORT

(2) Forward Demodulator Reports:

(a) PTE_DEMOD_PERFORMANCE_REPORT
(b) PTE_DEMOD_CONFIGURATION_REPORT

(3) Return Modulator Reports:

(a) PTE_MOD_CONFIGURATION_REPORT
(b) PTE_MOD_PERFORMANCE_REPORT

c. Redundant Bus Support - The TM shall provide support for a dual standby redundant bus (A side and B side) with redundant bus inputs (1 and 2) as shown in figure 13. Bus inputs are designated Bus A1, Bus A2, Bus B1 and Bus B2.

d. Remote Terminal Address - The remote terminal address for the A side data bus is contained in the cable connected to J109. The remote terminal address for the B side data bus is contained in the cable connected to J111. See table II and figure 13.

e. Data Bus Rules - Additional rules and details of data bus operation are contained in STGT-HE-06-2.

f. Signal Characteristics and Unit Interface - See table VII.

3.1.2.2.2.1 Data Bus Commanding - In addition to the descriptions of MIL-STD-1553B data bus commands provided in STGT-HE-06-2, the following requirements apply to commanding the unit. Commands may also originate from the front panel, when specified.

3.1.2.2.2.1.1 Synchronous Commands - Execution of synchronous commands shall be initiated by the TM at the 1 pps mark in the time field of the command (1 pps mark and CTFS 1 PPS epoch are synonymous). For this requirement, execution time is measured from the effective time. For commands that are to be completed and latched at the 1 pps mark, the execution time is specified as zero. The unit shall perform all necessary setup within the limits specified below.

a. Setup Time - Setup time shall be less than or equal to 1 second for all synchronous commands. Setup time is defined as the maximum time required to prepare for execution of a synchronous command.

b. Single Command Execution - The unit shall be capable of executing one synchronous command per effective time. Any subsequent command shall take precedence, and cancel the previous command.

c. Command Execution - The unit shall complete any necessary setup and execute the command within the time specified in table VIII.

3.1.2.2.2.1.2 Asynchronous Commands - Asynchronous commands are defined as commands which do not require an effective time. These commands shall be executed within the limits specified in table VIII, where execution time is measured from the receipt of the command at the unit.

a. Individual Command Rate - The unit shall support a command rate for any asynchronous command defined as one per execution time. The unit may overwrite the previous command of the same type.

b. Command Rate - The unit shall be capable of processing a minimum of four asynchronous commands sent to the unit within any one second period.

3.1.2.2.2.2 Operating States - With respect to logical commanding, and logical operation, the unit shall possess the following operating states. Test Modem operating states are described within two major MODEM operating modes. These modes are the PTE COHERENT mode and the PTE NONCOHERENT mode (not to be confused with coherent and noncoherent services). The PTE_GENERAL_CONFIGURATION_COMMAND instructs the unit which mode to configure.

a. PTE NONCOHERENT Mode - The PTE NONCOHERENT mode describes the operation mode where the Forward Demodulator and the Return Modulator are treated as separate units. The frequency sources in the Forward Demodulator and the Return Modulator are independent of each other (although they both are related to the CTFS).

b. PTE COHERENT Mode - The PTE COHERENT mode describes the operation mode where the Return Modulator frequency references for code and carrier are coherently related to Forward Demodulator frequency references for code and carrier.

c. State Diagrams - Within the PTE COHERENT and the PTE NONCOHERENT modes, there a several state diagrams. In the PTE NONCOHERENT mode there are the Demodulator States and the Modulator States. In the PTE COHERENT MODE there is only one state diagram.

d. Command State Table - Permissible commands are related to operating states. The command state table is given in table IX.

3.1.2.2.2.2.1 Common States - Common states are those states that are common to both Forward and Return. They are:

a. CONFIDENCE TEST IN PROGRESS - This state is entered upon power-up or reset of the unit. During this state the unit will be executing Confidence Test and will not respond to the data bus.

b. EXTENDED BIT - This state is entered by a PTE_SET_STATE_ COMMAND by setting the INITIALIZATION TYPE parameter to RUN EXTENDED BIT.

3.1.2.2.2.2.2 Demodulator States - Demodulator states are those states which are related to the Forward Demodulator. They are:

a. STANDBY - This state is entered upon completion of the Confidence Test, or by data bus command. This state indicates that the unit is ready to be configured.

b. DEMOD CONFIGURATION IN PROGRESS - This is a transition state between STANDBY and DEMOD CONFIGURED. This state indicates that the unit is dedicated to configuration of the unit. No signal acquisition or tracking will be done while in this state.

c. DEMOD CONFIGURED - The unit completes the DEMOD CONFIGURATION IN PROGRESS after it has received and processed the following commands:

(1) PTE_GENERAL_CONFIGURATION_COMMAND
(2) PTE_DEMOD_COMMON_CONFIGURATION_COMMAND
(3) PTE_DEMOD_SPECIFIC_CONFIGURATION_COMMAND.

The state transition will be complete within two seconds of receipt of these commands.

d. ACQUISITION - This state indicates that the Forward Demodulator is attempting to acquire the signal as configured. Any reconfiguration command during this state will transition the unit back to CONFIGURATION IN PROGRESS. Upon achieving carrier and code lock, the unit will transition to TRACK.

e. TRACK - This state indicates that the unit has achieved lock and is tracking the signal as configured. This state is the only state in which the Tracking Report parameters in the PTE_GENERAL_STATUS_REPORT are valid.

3.1.2.2.2.2.3 Modulator States - Modulator states are those states which are related to the Return Modulator. They are:

a. STANDBY - This state is entered upon completion of the Confidence Test, or by data bus command. This state indicates that the unit is ready to be configured.

b. MODULATOR CONFIGURATION IN PROGRESS - This state indicates that the Return Modulator is dedicated to the configuration of the unit. The Return Modulator is configured by the bus controller via the data bus commands PTE_GENERAL_ CONFIGURATION_COMMAND and PTE_MOD_CONFIGURATION_COMMAND.

c. MODULATOR CONFIGURED - After the receipt of the PTE_MOD_ CONFIGURATION_COMMAND and the PTE_GENERAL_CONFIGURATION _COMMAND the unit transitions to MODULATOR CONFIGURED. The transitions will be complete in less than two seconds after receipt of the commands. When in this state, the unit is ready to receive the PTE_MOD_START_SERVICE_ COMMAND.

d. MODULATOR IN SERVICE - This state indicates that the unit has received the PTE_MOD_START_SERVICE_COMMAND and has started the configured modulation service.

3.1.2.2.2.2.4 Coherent/Noncoherent Mode States - The states described previously have the same definitions in PTE COHERENT and PTE NONCOHERENT mode. However, the states interact differently, base on mode. State transition diagrams are illustrated in figures 14, 15, and 16.

3.1.2.2.2.3 Forward Model

a. Effective Time - The PTE_DEMOD_COMMON_CONFIGURATION_ COMMAND will be effective at lease one second prior to the effective time of the PTE_DEMOD_START_PN_MODEL_ COMMAND.

b. Ephemeris Data - No ephemeris data shall be required to start the Forward Model.

c. Start Forward Model - The Forward Model may be started on in the DEMOD CONFIGURED state. The Forward Model must be started (via the PTE_DEMOD_START_PN_MODEL_COMMAND) prior to the receipt of the PTE_DEMOD_START_ACQUISITION_COMMAND, so that the Forward Demodulator may use the PN code state provided in the Forward Model to assist acquisition.

d. New Commands - Receipt of a new PTE_DEMOD_START_PN_MODEL_ COMMAND shall cause the Forward Model to restart and synchronize with the new effective time.

3.1.2.2.2.4 Reconfigurations - A reconfiguration will cause the TM (Forward Demodulator and/or Return Modulator) to return to the applicable configured state (DEMOD CONFIGURED, MODULATOR CONFIGURED). A new start command (PTE_ DEMOD_START_ACQUISITION_COMMAND or a PTE_MOD_START_SERVICE_ COMMAND) is required to begin processing following a reconfiguration.

3.1.2.2.2.5 Command Memory - The unit shall provide memory capability for the PTE_DEMOD_SPECIFIC_CONFIGURATION_COMMAND, the PTE_DEMOD _COMMON_CONFIGURATION_COMMAND and the PTE_MOD_CONFIGURATION _COMMAND sufficient to allow null commands (no bits set in the applicable bit map) to be sent to transition from one state to the next, provided the applicable data were supplied during a previous command transmission. The unit shall use data from this last transmission to perform any necessary configurations.

3.1.2.2.2.6 Status Reporting and Time Tagging - Unit status shall be collected and available for report once per second and time tagged to the CTFS 1 PPS epoch. Status reports types and collection requirements are:

a. Integrated Status - Status reflecting performance over the entire one-second time period (t_0-1) to t_0 is called integrated status. This includes lock status and Doppler frequency status.

b. Snapshot Status - Status sampled at the CTFS 1 PPS epoch reflecting equipment state or a measurement at the instant, t_0, is snapshot status. This shall include status that reflects a synchronous command with an effective time of t_0, as well as status that reflects an asynchronous command which took effect within the previous one second.

c. Report Collection - Status reports time tagged, t_0, shall be available for collection by the data bus throughout the interval

   (t_0 + 400 ms) to (t_0 + 1 second)

   as illustrated in figure 17.

3.1.2.2.2.7 Ephemeris Downloading

a. Ephemeris - The term, ephemeris, shall be used to refer to frequency and delay profiles provided to the Test Modem via the data bus in the PTE_EPHEMERIS_DATA_COMMAND.

b. 10-10-10 Rule - Ephemeris downloaded shall follow the 10-10-10 rule: The unit shall apply newly downloaded ephemeris data within ten seconds after receipt, provided the data tables are received at a rate not to exceed ten minutes of ephemeris data in any ten second interval.

c. No Ephemeris Loaded - If no ephemeris data has been downloaded, the unit shall assume zero Doppler and zero range.

d. Other Commands - Other commands may be received during ephemeris data download. Whether or not they are accepted and/or processed depends only on the command state table.

e. Ephemeris Rejected - Ephemeris data shall be rejected by the unit if the TIME OF FIRST DATA parameter in the PTE_ EPHEMERIS_DATA_COMMAND is greater than sixty minutes in the future.

f. Capacity - The unit shall be capable of storing up to fifty minutes of ephemeris data. If, at any time, the unit runs out of ephemeris data, it shall continue to use the most recent data points it does have (by time tag, not by receipt time), until new data are provided.

3.1.2.2.3 Common Time and Frequency System (CTFS) - The unit shall receive and utilize for timing reference the following CTFS inputs from the Primary Interface:

a. CTFS 10 MHz
b. CTFS 1 Pulse per Second (1 PPS)
c. CTFS Time of Year (TOY)

3.1.2.2.3.1 CTFS 10 MHz - The signal characteristics and unit interface requirements are given in table X.

3.1.2.2.3.2 CTFS 1 PPS - The signal characteristics and unit interface requirements are given in table XI.

3.1.2.2.3.3 CTFS TOY - The signal characteristics and unit interface requirements are given in table XII.

3.1.2.2.3.4 Relationship Between 10 MHz and 1 PPS - The 10 MHz and 1 pps CTFS signals are coherent in frequency. That is, there are exactly 10 million cycles of the 10 MHz signal between successive leading edges of the 1 pps pulses. However, the signals are unsynchronized in the sense that the leading edge of the CTFS 1 PPS pulse is not necessarily aligned with a zero crossing of the CTFS 10 MHz sinusoid.

3.1.2.2.3.5 Leap Year and Second - The unit makes no special provisions for leap year or leap second. The unit accepts ephemeris data and processes it sequentially from the receipt of the data.

a. Leap Year - In the case of leap year, the unit sequences on a twenty four hour cycle and no special operations procedures are required.

b. Leap Second - In the case of leap second, implementation of a leap second durir a service will result in a time bias in the ephemeris file and in synchronous commands. This may require special operations procedures.

c. Implications - Leap year has no effect on unit tracking or data services. Leap second has no effect on unit data processing (except for synchronous reconfiguration commands). Tracking services may contain anomalies if the time bias is no managed operationally.

3.1.2.2.4 PTE 370 MHz IF Output - The Return Modulator shall be designed to provide a 370 MHz IF output, either modulated or unmodulated, as commanded, to the Primary Interface. The TM shall have the unit interface requirements and provide an IF signal having the characteristics listed in table XIII.

3.1.2.2.5 PTE 8.5 MHz IF Output - The Return Modulator shall be designed to provide a modulated 8.5 MHz IF output to the Primary Interface. The TM shall have the unit interface requirements and provide a modulated IF signal having the characteristics listed in table XIV.

3.1.2.2.6 PTE Baseband Data/Clock Inputs - The Return Modulator shall be designed to receive I and Q channel data and clock inputs for dual channel modes, or I channel data and clock for single channel modes, from the Primary Interface. These signals are also called Recovered I and Q Channel Data and Clock Inputs. Signal characteristics and unit interface requirements for these signals are listed in table XV.

3.1.2.2.7 PTE Baseband Command Data/Clock Outputs - The Forward Demodulator shall be designed to provide Command Channel Data and Clock Outputs to the Primary Interface. The TM shall have the unit interface requirements and provide baseband outputs having the characteristics as listed in table XVI.

3.1.2.2.8 PTE Low Data Rate Baseband Data Outputs - The Return Modulator shall be designed to provide I channel data and clock outputs to the Primary Interface after the commanded processing: data formatting, convolutional encoding, symbol formatting, interleaving, and PN spreading. The TM shall have the unit interface requirements and provide baseband outputs having the characteristics listed in table XVII.

3.1.2.2.9 I and Q Simulated User Return Data and Clock Inputs - The Return Modulator shall be designed to receive I and Q data and clock signals from the Primary Interface. This simulated data is also called external data in that it does not originate in the PTE. Signal characteristics and unit interface requirements for these signals are listed in table XVIII.

3.1.2.2.10 Recovered Forward Data and Clock Outputs - The Forward Demodulator shall be designed to provide Recovered Forward Data and Clock outputs to the Primary Interface. These signals are also known as Command Channel Received Data and Clock outputs. Signal characteristics and unit interface requirements for these signals are listed in table XIX.

3.1.2.2.11 PTE 370 MHz IF Input - The Forward Demodulator shall be designed to receive a modulated 370 MHZ IF input from the Primary Interface. Signal characteristics and unit interface requirements for this signal are listed in table XX.

3.1.2.3 Test Equipment Interface

3.1.2.3.1 Transmit Clock Outputs - The TM shall be designed to transmit three data clock signals:

a. Command Channel Transmit Clock Output
b. I Channel Transmit Clock Output
c. Q Channel Transmit Clock Output

3.1.2.3.1.1 Independent Clocks - The Forward Demodulator shall provide a Command Channel Transmit Clock Output to the Test Equipment Interface for use by the Forward Command Channel BERTS. The Return Modulator shall provide I and Q Channel Transmit Clock Outputs to the Test Equipment Interface for use by the Return I and Q Channel BERTS. For the Transmit Clock Outputs, the TM shall have the unit interface requirements listed in table XXI. The clocks shall be output on three separate ports on the unit to accommodate clocking the three BERTS independently.

3.1.2.3.2 <u>Data Inputs</u> - The TM shall be designed to receive three data input signals from the Test Equipment Interface:

a. Command Channel Data Input
b. I Channel Data Input
c. Q Channel Data Input

Signal characteristics and unit interface requirements for these signals are provided in table XXII.

3.1.2.3.3 <u>Recovered Data and Clock Outputs</u> - The TM shall be designed to provide the Test Equipment Interface with three recovered data and data clock signal pairs:

a. Command Channel Received Data and Clock Outputs
b. I Channel Received Data and Clock Outputs
c. Q Channel Received Data and Clock Outputs

Signal characteristics and unit interface requirements for these signals are provided in table XXIII.

3.1.2.3.4 <u>Test Modem 70 MHz IF Output</u> - The Return Modulator shall be designed to provide the Test Equipment Interface with a modulated 70 MHz IF output signal with the characteristics and unit interface requirements listed in table XXIV.

3.1.2.3.5 <u>Test Modem 70 MHz IF Input</u> - The Return Modulator will be designed to receive a modulated 70 MHz IF input signal with the characteristics and unit interface requirements listed in table XXV.

3.1.2.3.6 <u>IEEE-488 Data Bus</u> - The TM shall be designed to control and gather status from the test equipment listed in 3.1.2.d.

3.1.2.3.6.1 <u>Commands and Status</u> - Test Equipment commands and status capabilities are described in the maintenance and operation manuals furnished with the test equipment listed in 3.1.2.d.

3.1.2.3.6.2 <u>IEEE-488 Connector</u> - The TM shall have a standard IEEE-488 connector located on the unit back panel to interface with the Test Equipment Interface. The mating plug and cabling will be provided by the Test Equipment Interface.

3.1.2.4 <u>Controls, Indicators, and Test Points</u> - To support maintenance and operation of the unit, controls, indicators, and test points are provided on the front panel of the unit and on a maintenance panel. For switches with mechanical positions, the position will provide an indication of status. AC power shall be indicated by switch position and by a status lamp.

3.1.2.4.1 <u>Controls</u> - Controls are provided on the front panel and on the maintenance panel.

a. <u>Front Panel</u> - The unit shall have the following front panel controls:

(1) AC Power On/Off
(2) Local/Remote Switch
(3) Display Panel, also an indicator

b. <u>Maintenance Panel</u> - A reset switch shall be provided on the maintenance panel.

c. <u>Remote/Local</u> - The following requirements apply to local control of the Test Modem from its front panel:

(1) A Local/Remote selector switch on the front panel shall enable an operator to gain local control of the TM, or to relinquish control to the 1553 Bus. Selection or relinquishment of local control shall be possible only from the front panel.

(2) When in Remote mode, the TM shall respond only to commands provided over the 1553 Bus, and not to front panel controls, except those for status display and for Local/Remote selection.

(3) When in Local mode, the TM shall respond only to front panel controls, and not to commands provided over the 1553 Bus, except for status requests.

(4) Extended Bit shall be commandable from the front panel when the TM is in local mode.

(5) All status shall be available at the TM front panel, regardless of whether local or remote mode is selected.

(6) All status shall be provided over the 1553 Bus, upon command from the Control HWCI, regardless of whether local or remote mode is selected.

(7) Changing from local mode to remote mode, or remote to local, shall not alter the configuration state of the unit.

3.1.2.4.2 <u>Indicators</u> - Indicators are provided on the unit's front panel.

a. <u>Display</u> - An interactive touch panel display is provided on the front panel. The panel is capable of displaying 480 alphanumeric characters in a 12 line by 40 character format.

b. <u>Power Supply Status</u> - Indicator lamps provide a positive indication for each of the following power supplies:

(1) Primary AC Power
(2) + 5 volts DC
(3) + 5 volts DC (RF supply)
(4) + 12 volts DC
(5) + 15 volts DC
(6) - 5.2 volts DC
(7) - 12 volts DC
(8) - 15 volts DC

c. <u>Unit Status</u> - The following indicator lamps provide unit status:

(1) Normal
(2) Fault
(3) Test

d. Switch Positions - Switch position shall be used to indicate AC power on or off, and to indicate local or remote status.

3.1.2.4.3 Test Points - Test points are provided on the front panel and on the maintenance panel.

a. Front Panel - A test point to monitor the forward service IF test input to the Forward Demodulator is provided.

b. Maintenance Panel

(1) Power Supplies:

Primary AC Power
+ 5 volts DC
+ 5 volts DC (RF supply)
+ 12 volts DC
+ 15 volts DC
- 5.2 volts DC
- 12 volts DC
- 15 volts DC

(2) Test Signals:

PN Forward Epoch
PN Return Epoch
PN Code Acq
PN Code Trk
1 PPS Int1
1 PPS Int2
1 PPS Ext
DMSS
AGC
10 MHz
8.5 MHz Out
370 MHz Out

3.1.2.4.4 Jitter Test Points - Contractor defined test points for jitter testing are provided at J113 and J114 on the unit back panel.

3.1.2.4.5 Use and Limitations - The use and limitations of contractor defined controls indicators and test points will be further defined in SDRL OP-06. Nominal signal levels are also provided, where applicable.

3.1.3 Major Components List
The components of the TM are listed in IEC Drawing Number 7472506. The major components are:

a.	7473000	Timing Generator PWA (2 each)
b.	7473100	Demodulator Symbol/Synchronizer PWA
c.	7473200	Acquisition Processor PWA
d.	7473300	Pseudo-Noise Processor PWA
e.	7473600	Modem Control Processor PWA
f.	7473700	IEEE-488 Interface PWA

g. 7473900 Test Data Interface PWA
h. 7474300 RF Downconverter 2. PWA
i. 7474600 Synthesizer PWA (2 each)
j. 7475000 Test Modulator PWA
k. 7476100 Demodulator Processor PWA
l. 7510400 External Clock Synchronizer PWA

PWA stands for printed wiring assembly.

3.1.4 <u>Government Furnished Property List</u>
The unit neither requires nor contains any Government furnished property.

3.1.5 <u>Government Loaned Property List</u>
The unit neither requires nor contains any Government loaned property.

3.2 <u>Characteristics</u>

3.2.1 <u>Performance</u>
This section provides the performance characteristics of the Test Modem (TM). The unit shall perform the functions stated over the limits specified.

3.2.1.1 <u>Forward Demodulator</u> - This section provides the performance characteristics of the Forward Demodulator portion of the Test Modem.

3.2.1.1.1 <u>Signal Formats, Parameters and Constraints</u> - The unit shall receive and process all User Service Subsystem (USS) forward signals for all S-Band Single Access Forward (SSAF) including S-Shuttle Forward (SSHF), K-Band Single Access Forward (KSAF) including K-Shuttle Forward (KSHF), and Multiple Access Forward (MAF) services in support of preservice and end-to-end test (EET) functions. Necessary details of signal formats, parameters and constraints for forward service signals over which performance is specified are provided in the body of this specification. Specific details of all applicable USS forward signals are described in Appendix I. Refer to STGT-HE-04-05, -07, and -10 for complete signal definition and requirements.

3.2.1.1.1.1 <u>Input User Signals</u> - The unit will support input forward service signals at a nominal 370 MHz intermediate frequency. The unit shall perform demodulation, data recovery, and limited tracking service functions for all forward services (SSAF, SSHF, KSAF, KSHF, and MAF). The Forward Demodulator will be used to perform loopback tests on a Modulator/Doppler Predictor (MDP). Two loopback modes will be employed; (1) internal test loops, and (2) end-to-end tests.

a. <u>Internal Test Loops</u> - For internal test loops, the forward service signal from the MDP is routed to the TM Forward Demodulator without leaving the ground terminal. That is, it is looped back.

   (1) <u>Two Internal Loops</u> - The test loop may be either a short loopback (looped at IF) or an intermediate loopback (looped at RF) as shown in figures 1, 2, and 3. The unit does not distinguish between these two different configurations, although it may be commanded differently to accommodate the IF and RF frequency plan.

   (2) <u>Minimum C/No</u> - The minimum C/No for internal test loops will be 100 dB-Hz.

b. End-to-End tests - For end-to-end tests, the forward service signal from the MDP is transmitted to the Tracking and Data Relay Satellite (TDRS) on the space to ground link terminal (SGLT) antenna and returned to an end-to-end test (EET) antenna at the ground terminal via the selected user antenna on the TDRS.

(1) Added noise - Noise is added by the TDRS on the uplink signal and by the STGT EET low noise amplifiers (LNA) on the downlink.

(2) Minimum C/No - The minimum C/No for EET will be as specified in 3.2.1.1.1.2.3 Signal to Noise Ratio.

3.2.1.1.1.2 Parameters and Constraints - Specified performance is required for USS forward signals described in Appendix I, with the signal distortions and constraints listed below. The unit shall deliver specified performance within these boundaries.

3.2.1.1.1.2.1 Required Signal Energy - The unit shall provide specified performance when input signals possess the following signal plus noise power, signal to noise ratios, and C/No variations.

3.2.1.1.1.2.2 Signal Plus Noise Power - Input signal plus noise power at the 370 MHz IF input varies according to service (SSAF, SSHF, KSAF, KSHF, and MAF) as follows:

a. For SSAF, SSHF, and MAF - The input power at the 370 MHz IF input will be as follows:

(1) EET: -25.5 dBm, +/- 6 dB in a 50 MHz reference bandwidth centered about 370 MHz.

(2) Internal Loopback: -29 dBm, +/- 9 dB with a C/No greater than 100 dB-Hz.

(3) Spurious Signals: The total RSS value of all spurious signals within a 50 MHz bandwidth centered about 370 MHz will be -30 dBc, maximum; no single spurious signal will exceed -40 dBc.

b. For KSAF and KSHF - The input power at the 370 MHz IF input will be as follows:

(1) EET: -25.5 dBm, +/- 6 dB in a 100 MHz reference bandwidth centered about 370 MHz.

(2) Internal Loopback: -29 dBm, +/- 9 dB with a C/No greater than 100 dB-Hz.

(3) Spurious Signals: The total RSS of all spurious signals within a 100 MHz bandwidth centered about 370 MHz will be -30 dBc, maximum; no single spurious signal will exceed -40 dBc, maximum.

3.2.1.1.1.2.3 Signal to Noise Ratio - Forward service signal to noise ratio is provided in terms of C/No, where C is the received carrier power and No is the noise power, referenced to a one Hz bandwidth. Input C/No requirements are expressed in terms of achievable data rate (ADR) referenced to a given probability of error and implementation loss. The following formula shall determine the necessary C/No, and hence, the minimum signal energy required to obtain the achievable data rate, Rb.

The bit error probability acheived by the PTE FWD Demodulator shall be Pe or less provided the C/No at the IF input to the PTE FWD emodulator (Command Channel C/No for non shuttle services and total C/No for shuttle services) is greater than or equal to C/No as given by:

C/No = Eb/No(req) + 10logRb

where, Eb/No(req) is the specified minimum Eb/No at the IF input required to meet the specified bit error rate performance. Eb/No(req) may be written as,

Eb/No(req) = Eb/No + L[P_E,Rb] + L(A)

where:

a. All values are in decibels.

b. Eb/No is the theoretical value for the reference probability of error, P_E, at the referenced ADR operating point. Values are specified for P_E equal to 10^{-5}, 10^{-6}, and 10^{-7}.

c. L[P_E,Rb] is the allowable implementation loss for the given data channel and operating condition. Rb is the channel bit rate. P_E is the reference probability of error (also known as bit error rate). L[P_E,R_b] for all forward services are listed in table XXVI. This requirement applies only after signal tracking has been achieved.

d. L(A) is an additional implementation loss, if applicable, allowed for a particular mode of operation (e.g., 0.5 dB loss is allowed when PN spreading is used).

e. To satisfy the requirements for achievable data rate (ADR), the C/No of the IF input must be greater than or equal to the amount required to satisfy the equality at the given data rate, Rb.

3.2.1.1.1.2.4 C/No Variations - C/No may vary during end-to-end test support as follows:

a. Dynamic Range - The C/No may range from - 3 dB to + 12 dB relative to the reference C/No for $P_E = 10^{-5}$ for the FORWARD DATA RATE given in the PTE_DEMOD_SPECIFIC_CONFIGURATION_ COMMAND.

b. Variation Rate - The input C/No variation will not exceed 1 dB/second.

c. Internal Loopback - For internal loopback C/No is greater the 100 dB-Hz for all modes.

3.2.1.1.1.2.5 Data Rates - Data rates will be provided in the FORWARD DATA RATE parameter in the PTE_DEMOD_SPECIFIC_CONFIGURATION _COMMAND.

a. Accuracy - The actual data rate will be within +/- 0.1 percent of the commanded data rate.

b. Data Rate by Service - The permissible data rate ranges for service and mode are given in appendix I.

3.2.1.1.1.2.6 Symbol Transition Density - Requirements for Symbol Synchronization apply when the input symbol transition density satisfies the following criteria: Within any sequence of 512 symbols (symbols are bits for uncoded operation), the number of transitions will be greater than or equal to 128 and the maximum number of consecutive symbols without a transition will be less than or equal to 64.

3.2.1.1.1.2.7 Symbol (Data) Jitter - The clock timing jitter will be less than or equal to 0.5% of the symbol rate, three sigma.

3.2.1.1.1.2.8 Signal Distortions - The TM shall meet all acquisition, tracking and bit error rate requirements with input signals possessing the following types and amounts of distortions. Definitions for these parameters are described in STDN No. 101.2 Revision 6, Appendix I.

a. Phase Noise: As specified in table XXVII.

b. Gain Non-Flatness: The reference bandwidths are centered about 370 MHz.

(1) SSAF: 0.6 dB peak to peak over a 14 MHz bandwidth

(2) SSHF: 0.6 dB peak to peak over a 14 MHz bandwidth

(3) KSAF: 0.6 dB peak to peak over a 35 MHz bandwidth

(4) KSHF: 0.6 dB peak to peak over a 35 MHz bandwidth

(5) MAF: 0.6 dB peak to peak over a 4.2 MHz bandwidth

c. Phase Non-Linearity: The reference bandwidths are centered about 370 MHz.

(1) SSAF: 6 degrees peak to peak over a 14 MHz bandwidth

(2) SSHF: 6 degrees peak to peak over a 14 MHz bandwidth

(3) KSAF: 6 degrees peak to peak over a 35 MHz bandwidth

(4) KSHF: 6 degrees peak to peak over a 35 MHz bandwidth

(5) MAF: 0.6 degrees peak to peak over a 4.2 MHz bandwidth

d. MDP Distortions - As indicated within the MDP performance specification, 7472306.

(1) Gain Flatness
(2) Gain Scope
(3) PN code item
(4) Spurious Phase Modulation (PM)
(5) Incidental Amplitude Modulation (AM)
(6) Carrier Suppression
(7) Signal to thermal noise ratio

3.2.1.1.1.2.9 Radio Frequency Interference (RFI) - Not applicable.

3.2.1.1.1.2.10 IF Input Frequency Dynamics - The TM shall be capable of receiving and processing IF forward service signals with input frequency dynamics as specified in table XXVIII.

3.2.1.1.1.2.11 KSA Autotrack - Not applicable.

3.2.1.1.1.3 Frequency and Delay Profiles - The unit will be provided with ephemeris data to aid in acquisition and tracking.

a. Forward model Doppler compensation profile - The Forward Demodulator will be provided with the information necessary to construct a Doppler compensation frequency profile, $f_{DC}(t)$.

(1) Format - The profile is the sum of three components:

$$f_{DC}(t) = 370.\underline{0}\ \text{MHz} + df_F + df_{DC}(t)$$

where

(a) 370.0 MHz is a constant base frequency. (The underscore indicates that the final zero is repeated to the accuracy of the CTFS 10 MHz.)

(b) df_F is the FORWARD IF OFFSET FREQUENCY, provided in the PTE_DEMOD_COMMON_CONFIGURATION_COMMAND. The range of this parameter is:

SSAF and SSHF	-750 kHz to -250 kHz
KSAF and KSHF	-700 kHz to +700 kHz
MAF	1,300 kHz to 1,500 kHz

(c) $df_{DC}(t)$ is PTE DEMOD FORWARD MODEL DOPPLER COMPENSATION TABLE provided in the PTE_ EPHEMERIS_DATA_COMMAND. The entries in the table are values space at half second intervals aligned with the epochs of the CTFS 1 PPS reference. Linear interpolation is assumed between points.

(2) Profile Limits - The limits on the frequency profile are given in table XXX.

b. Delay Profile - The Forward Demodulator will be provided with a profile of predicted round trip delay, $D_X(t)$, which is defined as the estimated total delay from the MDP to the TM of a signal arriving at the Forward Demodulator at time, t. That is, a signal transmitted by the MDP at time $[t-D_X(t)]$ arrives at the Forward Demodulator at time, t, within the accuracy of the prediction.

(1) Purpose - The predicted delay profile is provided to the unit for use in:

(a) predicting the PN code state for acquisition and tracking, in conjunction with the MDP Doppler compensation profile;

(b) resolving ambiguity in range measurement.

(2) Format - The delay profile, $D_X(t)$, will be provided in the PTE DEMOD DELAY TABLE in the PTE_EPHEMERIS_DATA_COMMAND. The table entries are given in nanoseconds at half second intervals aligned with the CTFS 1 PPS epochs.

3.2.1.1.1.3.1 Forward Demodulator Precorrection - The behavior of the input carrier frequency received by the TM is characterized differently depending on whether an internal loopback test or an end-to-end test is performed.

a. Internal Loopback - The predicted input carrier frequency profile, $f_{FD}(t)$, for internal loopback tests is:

$$f_{FD}(t) = f_{DC}(t) = 370.\underline{0}\text{ MHz} + df_F + df_{DC}(t)$$

b. End-To-End - The predicted input carrier frequency profile, $f_{FD}(t)$, for end-to-end tests is:

$$f_{FD}(t) = 370.\underline{0}\text{ MHz} + df_D$$

where df_D is the DEMOD IF OFFSET FREQUENCY contained in the PTE_DEMOD_SPECIFIC_CONFIGURATION_COMMAND. The range of this parameter is:

SSAF and SSHF	-250 kHz to +250 kHz
KSAF and KSHF	-100 kHz to +100 kHz
MAF	-100 kHz to +100 kHz

3.2.1.1.1.3.2 Accuracy of Profiles

a. Delay Profile - The accuracy of the delay profile will be plus or minus 2 microseconds for internal loops and plus or minus 32 microseconds for end-to-end testing. This applies to all services.

b. Frequency Profile - The accuracy of the delay profile will be to a value much less than plus or minus 1 Hz for internal loops for all services. For end-to-end tests the frequency profile accuracy will be plus or minus 100 Hz for all services except KSAF and KSHF. KSAF and KSHF will be accurate to plus or minus 200 Hz.

3.2.1.1.2 PN Code and Carrier Acquisition - For signals with both command and range PN codes, acquisition performance applies to command channel acquisition, unless otherwise specified.

3.2.1.1.2.1 Acquisition - Carrier and code (if applicable) acquisition time shall not exceed the values specified in table XXIX for the C/No values shown, where C/No is referenced to the unit's input IF. Acquisition time shall be measured from the receipt of the PTE_DEMOD_START_ACQUISITION_COMMAND to the time at which PN code (if applicable) and carrier phase lock are achieved. For PN code acquisition, the time to acquire includes the time required to search the PN code uncertainty. Acquisition shall be achieved within the specified time given the unit is provided with predicted user ephemeris as specified in 3.2.1.1.1.3 Frequency and Delay Profiles.

3.2.1.1.2.2 False Lock - During signal acquisition and tracking the Forward Demodulator shall protect against false carrier acquisition and false acquisition to code sidelobes.

3.2.1.1.2.3 Reacquisition - Not applicable.

3.2.1.1.2.4 Range Channel Requisition - When commanded, after acquisition of the command channel has be achieved for SSAF, KSAF, and MAF configurations for which PN modulation is applicable, the TM shall perform a reacquisition on the range channel. The reacquisition time, measured from the receipt of the PTE_DEMOD_RANGE_CHANNEL_REACQUISITION_COMMAND to the instant PN code lock is achieved, shall be no greater than 5 seconds. This requirement applies only for internal loop test conditions for which the C/No exceeds 100 dB-Hz.

3.2.1.1.2.5 Performance Reporting - The lock status of the carrier and code shall be reported in the LOCK STATUS parameter of the PTE_DEMOD_PERFORMANCE_ REPORT. The report shall indicate, when applicable, whether the range channel or the command channel is being tracked.

3.2.1.1.3 Symbol/Decoder Synchronization - This paragraph specifies the minimum required synchronization time for forward service modes. Synchronization performance shall be met under the jitter conditions specified in 3.2.1.1.1.8 Symbol (Data) Jitter and with the data transition density conditions defined in 3.2.1.1.1.7 Symbol Transition Density.

3.2.1.1.3.1 Symbol Synchronization with Uncoded Data - For uncoded services, the minimum symbol transition density and minimum C/No for P_E equal to 10^{-5}, the time to synchronization shall not exceed the values specified below:

a. 300/data rate (bps) for biphase symbols with 90 percent probability (KSHF)

b. 3,000/data rate (bps) for NRZ symbols with 90 percent probability (SSAF, MAF, KSAF)

c. 14400/data rate (bps) for rates greater then 6 Mbps w/90 percent probability (KSAF)

d. Synchronization Defined - Symbol synchronization shall be defined as having been achieved when the error rate for the next 1,000 bits is 0.001 or less.

3.2.1.1.3.2 Measurement Time - Symbol synchronization time shall be measured from the time carrier lock occurs until the time symbol synchronization is achieved.

3.2.1.1.3.3 Symbol/Decoder Synchronization Time For SSHF coded services, for minimum data transition density and the minimum C/No required for 10^{-5} P_E performance, the time to achieve joint symbol and decoder synchronization shall not exceed 1,300/data rate (bps) with 90 percent probability. Symbol synchronization is defined as having been achieved when the error rate for the next 1,000 decoded bits is 0.001 or less.

3.2.1.1.3.4 Performance Reporting - The lock status of the symbol synchronizer and, when applicable, the decoder lock status, shall be reported in the LOCK STATUS parameter of the PTE_DEMOD_PERFORMANCE_REPORT.

3.2.1.1.4 Data Recovery

3.2.1.1.4.1 Tracking Performance

3.2.1.1.4.1.1 Mean Time to Cycle Slip - The mean time between cycle slips in the tracking of the carrier shall be at least 90 minutes for 3 dB less C/No than required for P_E equal to 10^{-5}, or 37 dB-Hz, whichever is greater.

3.2.1.1.4.1.2 Mean Time to Bit Slip - Bit slippage requirements shall be met for all services at a reference C/No consistent with that required for 10^{-5}. This requirement shall be met under the jitter and jitter rate conditions specified in 3.2.1.1.1.2.5.

a. Normal Transition Density - The mean time to first bit slip in the unit's clock recovery loop shall be no less than 90 minutes, or 10^{+10} clock cycles, whichever is greater, at the reference C/No required for $P_E = 10^{-5}$. This requirement applies for transition densities of at least 40 percent for NRZ symbols and any transition density for biphase symbols.

b. Low Transition Density - For NRZ symbol transition density between 25 and 40 percent, the mean time to first bit slip shall be no less than 90 minutes, or 10^{+10} clock cycles, whichever is greater, for C/No 1.0 dB greater than the reference C/No required for $P_E = 10^{-5}$.

3.2.1.1.4.1.3 Dynamics Tracking - Not applicable.

3.2.1.1.4.2 Ambiguity Resolution

3.2.1.1.4.2.1 Data Channel Ambiguity - Not applicable.

3.2.1.1.4.2.2 Data Phase Ambiguity - Data phase ambiguity is the uncertainty where the logic sense of the data is either true or complemented. Data phase ambiguity shall be resolved only for SSHF services. Data phase ambiguity shall be resolved using the convolutional decoding process.

3.2.1.1.4.2.3 Data Delay Ambiguity - Not applicable.

3.2.1.1.4.3 Eb/No Estimation - The unit shall compute an estimate of the Eb/No for detected data (matched filter output), and report the one second average value when commanded. The estimation error shall not exceed +/- 0.5 dB for Eb/No values in the range of 2.0 dB to 12.0 dB. The one second average shall be provided in the Eb/No ESTIMATE parameter in the PTE_DEMOD_PERFORMANCE_REPORT.

3.2.1.1.5 Tracking Services

3.2.1.1.5.1 Range Delay Measurement - The unit shall provide range delay measurements when configured for SSAF, MAF, and KSAF services for which PN modulation is enabled, and when in an internal loopback configuration. Range delay measurement are not required for SSHF service, or for end-to-end test modes.

3.2.1.1.5.1.1 Description

a. The Forward Demodulator shall measure the code state of the received PN code, $C_{FD}(t)$, at every 1 PPS mark.

b. The Forward Demodulator shall compute and report range delay, $D(t)$, at every 1 PPS mark based on the measured code state. $D(t)$ is computed as the solution to the implicit equation:

$$C_{FD}(t) = C_{MDP}[t-D(t)]$$

where

$C_{MDP}(\tau)$ is the MDP code state at time τ, which the Forward Demodulator can determine from its Forward Model.

c. Ambiguity in the above equation shall be resolved by choosing the solution closest to the provided predicted delay, $D_X(t)$.

3.2.1.1.5.1.2 Random Error - The random error in the range delay measurement shall not exceed the values given below for the data rates indicated.

a. 100 bps to 1,000 bps - 16 nanoseconds, rms

b. Greater Than 1,000 bps - 8 nanoseconds, rms

3.2.1.1.5.1.3 Systematic Error - The residual systematic error contribution to the range delay measurement shall be less than or equal to +/- 5 nanoseconds over a one hour period.

3.2.1.1.5.1.4 Reporting - Measured range delay shall be available during the entire period from 400 milliseconds to 1,000 milliseconds following the 1 pps mark at which the measurement was made. All measurements shall be time tagged with the CTFS 1 PPS epoch time. The range delay measurement shall be reported in the RANGE DELAY parameter of the PTE_DEMOD_PERFORMANCE_REPORT.

3.2.1.1.5.2 Doppler Measurement - Doppler measurements shall be provided for all forward services for both internal and end-to-end test configurations.

3.2.1.1.5.2.1 Description - With $f_{FDi}(t)$ denoting the carrier frequency of the IF input as a function of time, then the unit shall compute a one second average Doppler, $\Delta(kT)$, where $\Delta(kT)$ is defined as:

$$\Delta(kT) = \int_a^b [f_{FDi}(u) - f_{FD}(u)]\,du$$

where,

a. Limits a and b

$a = (k-1)T$
$b = kT$

kT is the time of the kth 1 PPS mark

b. Carrier Frequency - $f_{FDi}(t)$ is the input carrier frequency; $f_{FD}(t)$ is the unit's estimate of the carrier frequency based on the profile derived from the ephemeris.

3.2.1.1.5.2.2 Measurement Error - The rms error of a one second average Doppler frequency measurement shall not exceed the limits specified below. This requirement applies when the C/No is consistent with P_E equal to 10^{-5}.

a.	100 bps to 500 bps	0.32 radian/second
b.	500 bps to 1,000 bps	0.24 radian/second
c.	> 1,000 bps	0.16 radian/second

The above allowed error values are in addition to the error introduced by the allowed +/- 25 nanoseconds of uncertainty on the 1 pps time reference.

3.2.1.1.5.2.3 Reporting - The Forward Demodulator shall compute and report Δ(kT) every second. This value, which is the measure of the difference between the actual measured frequency and the estimated frequency profile, is the parameter INTEGRATED DOPPLER FREQ in the PTE_DEMOD_PERFORMANCE_REPORT. The one second average Doppler count measurement shall be available during the entire period from 400 milliseconds to 1,000 milliseconds following the 1 pps mark at which the measurement was made. The measurement shall be time tagged with the 1 pps mark time.

3.2.1.1.6 Control of Test Equipment - When commanded, the unit shall, by controlling the Test Equipment Forward Command Channel BERTS, generate a pseudo-random test baseband data signal and synchronous clock as follows:

a. Frequency Range - The clock frequency shall be commandable from 100 Hz to 25 MHz with a resolution of 1 Hz.

b. Clock Accuracy - The Forward Demodulator shall generate a clock frequency with an accuracy of +/- 0.01 percent of the commanded frequency.

c. Clock Jitter - The clock jitter frequency shall be a maximum of 0.01 percent.

d. Sequence Length - The Forward Command Channel BERTS is capable of data sequences of period (2^n-1), for n equal to 5, 9, 11, 20, or 23. The value, n, shall be selectable by command to the Forward Demodulator.

3.2.1.1.6.1 Forward BER Measurement - The Forward Demodulator shall, when commanded via the PTE_DEMOD_START_FWD_BER_TEST_COMMAND, perform a bit error rate (BER) measurement on the recovered forward channel test data stream. This measurement is only required when the data is locally generated.

a. Response to Command - Upon receipt of the PTE_DEMOD_START_FWD_BER_TEST_COMMAND, the Forward Demodulator shall configure the Command Channel BERTS in the Second Test mode with parameters as commanded and commence BER measurement. Parameters are:

(1) Test Period - Test periods of up to 99,999 seconds may be selected with one second resolution. The test period is determined by the value for FWD TEST PERIOD in the PTE_DEMOD_START_FWD_BER _TEST_COMMAND.

(2) Test Interval - The unit shall permit BER measurement intervals for 10^3 to 10^{10} bits. Intervals are selected in powers of ten as determined by the value for the exponent provided in the FWD TEST INTERVAL in the PTE_DEMOD_START_FWD_BER_TEST_COMMAND.

b. Reporting - Test results are provided in the PTE_BER/TIC/Eb/No_ MEASUREMENTS_REPORT.

3.2.1.2 Return Modulator - The unit shall accept NRZ-L data with data rates ranging from 100 bps to 12 Mbps and provide PSK modulation within the limits specified for S-Band Single Access Return (SSAR), S-Band Shuttle Return (SSHR), K-Band Single Access Return (KSAR), K-Shuttle Return (KSHR), and Multiple Access Return (MAR) services. Data may be generated by the Test Equipment I and Q Channel BERTS, controlled by the TM, or data may be provided to the TM from an external source via the Primary Interface.

a. 1553B Data Bus Commanding - The configuration for the Return Modulator is provided in the PTE_MOD_CONFIGURATION _COMMAND.

b. I and Q Source Independence - I and Q channels shall be capable of independent configuration. That is, the data source for one channel may be external while the other channel data source is internal, and vice versa. Data source is controlled by the I DATA SOURCE and Q DATA SOURCE values in the PTE_MOD_CONFIGURATION_COMMAND. Unless otherwise specified, other I and Q channel parameters are also independent.

c. Synchronizing to External Data - The rate of external NRZ-L data and clock supplied to the unit will match the commanded rate to the accuracy of the CTFS. The Return Modulator shall synchronize its data processing to the input clock within 1,000 symbols after configuration is complete and data clock is present.

3.2.1.2.1 Data Processing Configurations and Modulation Formats - Necessary details of signal formats, parameters and constraints for return signals over which unit performance is specified are provided in the body of this specification. Specific details of all applicable USS return signals are described in Appendix I. Refer to STGT-HE-04-05, -07, and -10 for complete signal definition and requirements.

3.2.1.2.2 Data Generation - When indicated by the commanded configuration, the Return Modulator shall, using the Test Equipment BERTS, generate up to two (I and Q) independent pseudo-random test baseband data and synchronous clock signals, each of which independently satisfies the following requirements.

a. Clock Source - The unit shall generate the clocks required by the BERTS and output them independently (I and Q) to the Test Equipment Interface.

b. Frequency Range - The clock frequency shall be commandable from 100 Hz to 12 MHz with a resolution of 1 Hz. Clock frequency is controlled by the I DATA RATE and Q DATA RATE values in the PTE_MOD_CONFIGURATION_COMMAND.

c. Clock Accuracy - The generated clock frequency shall be within +/- 0.01 percent of the commanded frequency.

d. Clock Jitter - The clock jitter shall be a maximum of 0.01 percent.

e. Sequence Length - The Test Equipment BERTS are capable of generating pseudo-random data sequences of period (2^n-1) bits for n equal to 5, 9, 11, 20, or 23. The value of n shall be selectable and will be provided in the I BERT PN LENGTH and Q BERT PN LENGTH values in the PTE_MOD_CONFIGURATION_COMMAND.

f. Test Equipment Control - The unit shall provide the necessary control of the BERTS via the IEEE-488 data bus.

3.2.1.2.3 Data Formatting and Encoding - The unit shall provide data formatting, symbol formatting, convolutional encoding, and interleaving, as specified.

3.2.1.2.3.1 Data Formatting - Data format conversion shall take place before convolutional encoding or interleaving and will be explicitly commanded by the I DATA FORMAT and Q DATA FORMAT values in the PTE_MOD_CONFIGURATION_COMMAND. The Return Modulator shall be capable of providing the following format conversions of the input NRZ-L data:

a. NRZ-L to NRZ-L (no conversion)
b. NRZ-L to NRZ-M
c. NRZ-L to NRZ-S
d. NRZ-L to Biphase-L
e. NRZ-L to Biphase-M
f. NRZ-L to Biphase-S

3.2.1.2.3.2 Convolutional Encoding - The Return Modulator shall be capable of generating each of the following convolutional codes.

a. Code 1

(1)	Type:	Convolutional, non-systematic, transparent
(2)	Rate:	1/2
(3)	Constraint length:	k = 7
(4)	Generator functions:	G1 = 1111001 G2 = 1011011

(5) Symbols generated from G1 shall precede symbols generated from G2 relative to the data bit period.

(6) Symbols generated from G2 shall either be true or inverted as commanded.

b. Code 2

(1) Type: Convolutional, non-systematic, transparent

(2) Rate: 1/2

(3) Constraint length: k = 7

(4) Generator functions: G1 = 1011011
G2 = 1111001

(5) Symbols generated from G1 shall precede symbols generated from G2 relative to the data bit period.

(6) Symbols generated from G1 shall be inverted.

Inversion is implied by selection of Code 2; no further explicit commanding is required.

c. Code 3

(1) Type: Convolutional, non-systematic, transparent

(2) Rate: 1/3

(3) Constraint length: k = 7

(4) Generator functions: G1 = 1111001
G2 = 1011011
G3 = 1110101

(5) The symbols sequence for the convolutional coding shall be symbols generated from G1, G2, and G3 successively relative to the data bit period.

(6) Alternate symbols generated from the convolutional coding shall be inverted. Inversion is implied by selection of Code 3; no further explicit commanding is required.

d. Code 4

(1) Type: Convolutional, non-systematic, non-transparent

(2) Rate: 1/3

(3) Constraint length: k = 7

(4) Generator functions: G1 = 1111001
G2 = 1011011
G3 = 1100101

(5) The symbols sequence for the convolutional coding shall be symbols generated from G1, G2, and G3 successively relative to the data bit period.

(6) Inversion is not an option.

e. 1553B Data Bus Commanding - Code selection (with the exception of Code 4) will be explicitly selected in the PTE_MOD_CONFIGURATION_ COMMAND. Code 4 will be implied by the selection of SERVICE TYPE equal to SSHR, Mode 1 or 2. Generator inversion commanding is required to be explicit for Code 1. Inversion is implicit for G1 symbols in Code 2, and for alternate generator functions for Code 3. Inversion is not an option for Code 4.

3.2.1.2.3.3 Symbol Formatting - The unit shall provide the capability to convert encoded NRZ symbols to biphase symbols. Symbol conversion shall take place at the output of the encoder and will be explicitly commanded by the I SYMBOL FORMAT and the Q SYMBOL FORMAT values in the PTE_MOD_CONFIGURATION_COMMAND.

3.2.1.2.3.4 Interleaving - The Return Modulator shall perform interleaving as specified in STDN-101.2, Appendix J., with the following restrictions. Interleaving takes place after the encoders and is not used with symbol format conversion. Interleaving is explicitly commanded via the SETUP MISCELLANEOUS PARAMETERS in the PTE_MOD_ CONFIGURATION_COMMAND.

3.2.1.2.4 PN Code Generation - The Return Modulator shall be capable of generating the Mode 1, Mode 2, and Mode 3 Return Link Codes as specified in STDN No. 108.

3.2.1.2.4.1 PN Code Rate - See 3.2.1.2.6 Carrier Frequency and PN Code Rate.

3.2.1.2.4.2 PN Modulation - When PN modulation is required, the PN code applied to the I channel shall be modulo-2 added to the I channel symbol stream after all required data formatting, encoding, symbol formatting, and interleaving have been accomplished. Similarly for the Q channel, the PN code applied to the Q channel shall be modulo-2 added to the Q channel symbol stream after all required data formatting, encoding, symbol formatting, and interleaving have been accomplished.

3.2.1.2.5 PSK Modulation - The Return Modulator shall be capable of binary phase shift keying (BPSK) and quadrature phase shift keying (QPSK) modulation, including unbalanced QPSK (UQPSK) and staggered QPSK (SQPSK).

3.2.1.2.5.1 Modulator Performance - The Return Modulator shall satisfy the following signal parameters and constraints for modulator performance. The definitions for signal parameters are described in STDN No. 101.2 Revision 6, Appendix I, but are referenced at the Test Modem output (as opposed to HPA output referenced in STDN No. 101.2).

a. Carrier I:Q Relationship - For quadrature modulation formats, the in phase I channel will lead the quadrature Q channel by 90 degrees, +/- 3 degrees.

b. I:Q Power Ratio - The I channel to Q channel power ratio will be commandable to the values 4:1, 1:1, 1:2, and 1:4 to within +/- 0.4 dB of the commanded ratio.

3.2.1.2.5.2 Carrier to Noise Ratio - Carrier to Noise Ratio is defined in terms of C/No and a reference bandwidth.

a. C/No - Using the Eb/No Test Set in the Test Equipment, the Return Modulator shall be capable of setting the selected IF output to a C/No value in the range from 27 to 88 dB-Hz, commandable in 1 dB increments. Command value is determined by the parameter C/No SETTING in the PTE_MOD_CONFIGURATION_ COMMAND.

b. No Noise - The unit shall also provide the selected IF output with no noise added, according to the value of NOISE ON/OFF in the PTE_MOD_CONFIGURATION_COMMAND. When noise is commanded off, no noise is added by the Eb/No Test Set, regardless of the value for C/No SETTING.

c. Selected IF - The unit shall be capable of providing a 370 MHz IF or a 8.5 MHz IF according to the value of NOMINAL IF OUTPUT FREQ in the PTE_MOD_CONFIGURATION_ COMMAND.

d. 370 MHz Noise Bandwidth - When the PTE 370 MHz IF Output is selected, the output modulated IF plus noise shall be filtered to a 3 dB bandwidth of 30 MHz +/- 10 percent, centered at 370 MHz.

e. 8.5 MHz Noise Bandwidth - When the PTE 8.5 MHz IF Output is selected, the output modulated IF plus noise shall be filtered to a 3 dB lowpass bandwidth of 15 MHz +/- 10 per cent.

f. Setup Time and Calibration - The Test Equipment Eb/No Test Set may require setup time and calibration time that may limit the maximum time it takes to configure or reconfigure tests which require added noise.

3.2.1.2.6 Carrier Frequency and PN Code Rate - This section specifies the performance requirements for the output carrier frequency, $f_{RM}(t)$, and the PN code rate, $r_{RM}(t)$, generated by the Return Modulator. Carrier frequency and PN code rate are affected by Doppler compensation, user frequency and service assignment, and by the selected test loop. Additionally, carrier and code frequency depend on whether return test loop is coherent or noncoherent with the forward test loop.

3.2.1.2.6.1 Independently Generated Code and Carrier - For noncoherent test loops, the Return Modulator carrier frequency and code rate will be generated independently of the Forward Demodulator.

a. Frequency Profile - The Return Modulator will be provided with the information necessary to construct a profile of commanded output carrier frequency, $f_{RM}(t)$.

(1) Format - The frequency profile, $f_{RM}(t)$, is the sum of three components:

$$f_{RM}(t) = F_{IF} + df_M + df_{RM}(t)$$

where:

(a) F_{IF} will be either 8.5$\underline{0}$ MHz or 370.$\underline{0}$ MHz (the underscore indicates that the final zero is repeated to the accuracy of the CTFS). The value of F_{IF} is determined by the selection made for NOMINAL IF OUTPUT FREQ in the PTE_MOD_CON-FIGURATION_COMMAND.

(b) df_M is the RETURN MODULATOR IF OFFSET FREQUENCY contained in the PTE_MOD_ CONFIGURATION_COMMAND. The range of this parameter is:

SSAR and SSHR	-750 kHz to +250 kHz
KSAR and KSHR	-770 kHz to +770 kHz
MAR	-100 kHz to +100 kHz

(c) $df_{RM}(t)$ is a profile of deviation frequency versus time, which will be provided to the TM as a table of values spaced at 0.5 second intervals aligned with the epochs of the CTFS 1 PPS. Linear interpolation between the discrete values is assumed and shall be performed by the unit. The table of values is provided in the PTE MODULATOR FREQUENCY COMPENSATION TABLE contained in the PTE_EPHEMERIS_DATA_ COMMAND.

(2) Limits - The profile will conform to the limits given in table XXX.

(3) Storage Capacity - The unit shall be capable of storing up to 50 minutes of profile data.

(4) Profile Updating - The unit shall be capable of updating or overwriting stored profile data in response to command without affecting performance. Newly supplied profile data shall be implemented no later than 10 seconds after receipt.

b. IF Carrier Frequency - The unit shall generate an IF carrier which follows the commanded frequency with a series of phase continuous frequency steps.

(1) Update Rate - The unit shall be capable of a stepping rate of 500 steps per second, minimum.

(2) Accuracy - The unit shall follow the commanded profile to an accuracy of +/- 0.8 Hz.

c. PN Code Rate - The PN code rate, $r_{RM}(t)$, generated by the Return Modulator for noncoherent test loops shall be coherently related to the Return Modulator carrier frequency, $f_{RM}(t)$, in accordance with the following equation:

$$r_{RM}(t) = [f_{RM}(t) + f_{trl}] * [M/(N*Q)]$$

where:

(1)	$r_{RM}(t)$	=	PN Code Rate
(2)	$f_{RM}(t)$	=	Return Modulator output carrier frequency
(3)	f_{trl}	=	RETURN LOOP TEST TRANSLATION FREQUENCY provided in the PTE_MOD_CONFIGURATION_COMMAND
(4)	M	=	31
(5)	N	=	96
(6)	Q	=	240 for SSA and MA 1,600 for KSA

d. PN Code Synchronization - The Return Modulator shall synchronize the starting epoch of the I channel PN code with the CTFS 1 PPS epoch corresponding to effective time provided in the PTE_MOD_START_SERVICE_COMMAND.

e. Start of Modulation - Modulation of the IF carrier by PN code and data, as applicable, shall begin at the 1 PPS mark corresponding to the effective time provided in the PTE_MOD_START_SERVICE_COMMAND.

3.2.1.2.6.2 Dependently Generated Code and Carrier - For coherent test loops, the Return Modulator carrier frequency and PN code rate will be derived from the recovered carrier frequency and PN code rate from the Forward Demodulator.

a. IF Carrier Frequency - The Return Modulator output carrier frequency, $f_{RM}(t)$, shall be coherently derived from the IF carrier frequency recovered from the Forward Demodulator, $f_{FDi}(t)$, in accordance with the formula:

$$f_{RM}(t) = F_{IF} + [Q/P] * [f_{FDi}(t) - 370.0 \text{ MHz}]$$

where:

(1) The Constants P and Q - Q is the previously defined constant. Q is equal to 240 for SSA and MA; Q is equal to 1,600 for KSA. P is equal to 221 for SSA and MA; P is equal to 1,469 for KSA.

(2) F_{IF} is the previously defined NOMINAL IF OUTPUT FREQ.

b. PN Code Rate - For coherent test loops, the Return Modulator PN code rate and PN epoch shall be synchronized with the recovered PN clock and epoch from the Forward Demodulator.

c. Start of Modulation - For coherent test loops, modulation of the IF carrier by PN code and data, as applicable, shall begin automatically when the PTE Forward Demodulator achieves lock. No PTE_MOD_START_SERVICE command will be issued.

3.2.1.2.7. BER Measurement - In response to a PTE_MOD_START_ RTN_BER_TEST_COMMAND, the unit shall perform bit error rate (BER) measurements on the recovered test data stream. The unit shall use the Test Equipment Return I Channel BERTS and the Q Channel BERTS to make these measurements.

a. I and Q Independence - I and Q channels shall be capable of independent commanding.

b. Test Interval - The unit shall permit BER measurement intervals for 10^3 to 10^{10} bits. Intervals are selected in powers of ten as determined by the value for the exponent provided in RETURN I TEST INTERVAL and RETURN Q TEST INTERVAL in the PTE_MOD_START_RTN_BER_TEST_ COMMAND.

c. Test Period - Test periods of up to 99,999 seconds may be selected with one second resolution. The test period is determined by the values for RETURN I TEST PERIOD and RETURN Q TEST PERIOD in the PTE_MOD_ START_RTN_BER_COMMAND.

3.2.1.2.8 Data Delay Measurement - In response to a PTE_MOD_ MEASURE_TIME_INTERVAL_COMMAND, the unit shall measure the delay from the time an epoch of the pseudo-random test sequence leaves the selected I or Q channel BERTS transmitter to the time it arrives at the BERTS receiver. The results of the measurement shall be place in the PTE_BER/TIC/Eb/No_MEASUREMENTS_REPORT for collection by the data bus.

3.2.1.3 Performance Monitoring - The unit will provide additional performance monitoring functions in support of operational performance monitoring and to support maintenance. Descriptions of these tests are provided in STGT-HE-06-2.

3.2.1.3.1 Confidence Test - The unit shall provide a self-test capability which shall provide initial confidence in the unit. The test shall be run whenever the unit is initially powered up, or when commanded, and shall include the following:

a. Local/Remote Control - The test shall be initiated upon power up, by local control, or upon remote command.

(1) Local Control - The unit shall run Confidence Test when the Reset Switch located on the Maintenance Panel is depressed, regardless of whether the Local/Remote switch is in the Local or Remote position.

(2) Remote Control - When the Local/Remote switch is in the Remote position, the unit shall run Confidence Test upon receipt of the PTE_SET_STATE_COMMAND, with the INITIALIZATION TYPE set to RESET. This causes the unit to enter the operating state CONFIDENCE TEST IN PROGRESS.

(3) Test Indicators - During CONFIDENCE TEST IN PROGRESS the unit shall light the front panel unit status indicator, Test. If Confidence Test fails, the unit status indicator, Fault, shall be lighted. Upon successful completion of Confidence Test the status indicator, Normal, shall be lighted.

(4) Data Bus Response - While Confidence Test is in progress (the operating state CONFIDENCE TEST IN PROGRESS), the unit will not respond to data bus commands or report status.

3.2.1.3.1.1 Performance Requirements - The Confidence Test shall:

a. Detect Failures - The Confidence Test shall detect hard failures of power supplies and microprocessors for at least 95 percent of all failure modes, weighted for failure rate.

b. Report Failures - When a malfunction is detected, data concerning the malfunction shall be entered into temporary storage for later recall by the data bus via the PTE_GENERAL_STATUS_REPORT. Confidence Test data shall also be available on the unit Front Panel Display.

c. False Alarm - The Confidence Test shall have a maximum false alarm rate of one percent.

d. Test Time - The time between initiation of Confidence Test and the availability of test results via the data bus shall not exceed 10 seconds.

3.2.1.3.2 Additional Tests - To support maintenance and operation, the unit shall provide On-Line BIT and Extended BIT tests.

3.2.1.3.2.1 On-Line BIT - On-Line BIT is a continuous process that is run during all Test Modem operating states. Descriptions of On-Line BIT functions are provided in Appendix II.

3.2.1.3.2.1.1 Status Reporting - On-Line BIT results shall be provided in the PTE_GENERAL_STATUS_REPORT and on the Front Panel Display.

3.2.1.3.2.2 Extended BIT - Extended BIT, as its name suggests, is a more extended series of built in tests (BIT) that must be run when the unit is not supporting active user services. Results of Extended BIT shall provide sufficient data to the Subsystem Controller such that at least 75 percent of the possible faults identified in the FMEA, RMA-02, can be detected and isolated to an LRU or group of LRUs using solely the BIT results and the isolation logic contained in RMA-02.

3.2.1.3.2.2.1 Test Initiation and Termination - This test will be controlled via data bus command or by front panel command.

a. Data Bus Command - The unit shall initiate Extended BIT in response to the data bus command, PTE_SET_STATE_ COMMAND with the INITIALIZATION TYPE set to RUN EXTENDED BIT. Tests shall terminate upon receipt of a PTE_SET_ STATE_COMMAND with the INITIALIZATION TYPE set to HALT EXTENDED BIT, or upon completion of the Extended BIT tests.

b. Front Panel Command - The unit shall initiate Extended BIT in response to front panel command via selection on the Front Panel Display (touch panel). The unit must in Local mode for Extended BIT to be activated by front panel control. Tests shall terminate upon receipt of a subsequent front panel command, or upon completion of the Extended BIT tests. If mode is returned to Remote, the tests may be terminated by data bus command.

c. Test Completion - Extended BIT shall sequence through the test groups and will terminate upon completion. There is no time specified for test duration. Upon test termination, either by completion, or upon command, the unit shall return to the STANDBY operating state.

d. Test Groups - Test groups are described in STGT-HE-06-2.

3.2.1.3.2.2.2 Status Reporting - Extended BIT results shall be available in the PTE_EXTENDED_BIT_REPORT and on the front panel display.

3.2.1.3.2.3 Error Codes - Error codes are provided which provide the reason if the last data bus command was not accepted or executed.

3.2.2 Physical Characteristics
The unit shall be designed to be housed in a standard 19-inch RETMA rack. The unit shall be provided with slide hardware. Overall geometry and arrangement of major components and units shall provide for easy removal and replacement of units and components to minimize equipment maintenance downtime.

3.2.2.1 Dimensions - The dimensions of this unit are as follows:

a. Panel Height - 12.22 +0.00, -0.03 in.
b. Panel Width - 18.97 +0.00, -0.03 in.
c. Chassis Depth - 24 in., max.
d. Chassis Width - 17.75 in., max, including slides

3.2.2.2 Weight - The weight of this unit shall not exceed 85 pounds.

3.2.3 Reliability
The unit shall have a minimum Mean Time Between Failure (MTBF) goal of 2500 hours when operated in a fixed environmentally controlled area. The MTBF will be calculated using an average temperature of 75 degrees F.

3.2.3.1 Mean Time Between Failures - The MTBF requirements shall apply to the unit while being maintained in accordance with 3.2.4, and during exposure to the environments of 3.2.5. The MTBF shall be analyzed using failure rates based on MIL-HDBK-217, or other sources that are approved by the procuring activity. In order to achieve the required MTBF, the reliability program provisions of STDN 927.4, Section 6 shall apply.

3.2.3.2 Design Life - The unit shall be designed for a lifetime of ten (10) years of continuous operation, not including administrative periods of non-operation, or downtime for maintenance, as specified in 3.2.4 .

3.2.3.3 Acoustical Noise - The acoustical noise level with all fans and/or blowers on shall be in accordance with MIL-STD-1472 paragraphs 5.8.3.1 and 5.8.3.3.2.

3.2.4 Maintainability
The unit shall meet the maintainability requirements as defined in the following paragraphs.

3.2.4.1 On-Line Replacement - The unit shall be designed to support in-circuit repair or system restoration as defined in 3.5 by fault isolation, disassembly, failed item removal and replacement, reassembly, and test of the replaced unit at the line replaceable unit (LRU) level.

3.2.4.1.1 LRU Level Definition - The line replaceable unit level for the unit is board/module, or the unit in its entirety. LRU's shall incorporate status indicators along with test and monitoring points as appropriate to allow test via Maintenance Test Group (MTG) test equipment.

3.2.4.2 Mean Time To Repair (MTTR) - The unit shall be designed such that the mean time to achieve on-line repair, including isolation, removal, replacement, and retest of the LRU shall not exceed 25 minutes. In order to demonstrate achievement of the required MTTR, the maintainability verification provisions of STDN No. 927.2, Section 4.4.1.3 shall apply. Logistics time to obtain parts or test equipment is excluded.

3.2.4.3 Maximum Time To Repair (MTR) - The maximum time to effect on-line repair, as defined in 3.5.1.3, shall not exceed one hour for the 90th percentile of failures.

3.2.5 Environmental Conditions

3.2.5.1 Nonoperating Environments - This unit shall suffer no permanent degradation or damage when subjected to the following environments:

a. Temperature - From -20 to 160 degrees F.
b. Humidity - 0 to 100 percent relative humidity, non-condensing environment.
c. Altitude - Sea Level to 35,000 feet.
d. Solar Radiation - 350 BTU/ft^2/hour

3.2.5.2 Operating Environments - This unit shall meet all specified performance requirements while exposed to the following environments:

a. Temperature - From 50 to 100 degrees F.
b. Humidity - From 20 to 80 percent without condensation
c. Altitude - Sea Level to 12,000 feet

3.2.6 Transportability
The equipment shall be capable of shipment by ship, truck, rail, and air transport.

3.3 Design And Construction
Design and construction requirements shall be in accordance with MIL-STD-454 Guidelines, except as specified herein. Commercial equipment such as computers and their peripherals, test equipment, single-board computer boards, and compatible Input/Output (I/O) boards, etc., that meet the performance requirements for use on the program shall be exempt from these requirements.

3.3.1 Materials, Processes, and Parts

3.3.1.1 Materials - Corrosion-resisting materials and finishes shall be used to the maximum extent. Metal-to-metal contact of dissimilar metals shall be governed by the criteria of MIL-E-16400. Fungus nutrient materials, mercury, and radioactive material shall not be used in any form.

3.3.1.2 Standard and Non-Standard Parts and Materials - Parts and Materials shall be selected and fabricated or assembled in such a manner that they conform to these specifications. Non-standard parts and materials as defined shall be used only with the approval of GE Contracts Administration.

3.3.1.2.1 Standard Parts and Materials - Standard parts and materials shall be those specified by any of the following:

a. A published government qualified products list.

b. Mil-Std-975 Grade 2.

c. Commercial specifications certified by the vendor to meet industry specifications and standards as those promulgated by nationally recognized associations, and technical societies as having coordinated status with the government requiring activities.

d. Commercial parts certified by the vendor to meet industry specifications and standards having limited coordination status with the government requiring activities.

3.3.1.2.2 Non-Standard Parts and Materials - Non-standard parts and materials are defined as those being:

a. Selected parts, or those whose performance and physical characteristics are unique when compared with vendor stocked or cataloged items and which cannot be ordered by standard nomenclature only.

b. Any parts and materials not covered by the standard parts and materials definition.

3.3.1.2.3 Standard Components - Standard commercial components shall be employed throughout, to the greatest extent practicable. Sole source components shall be held to a minimum. Unless approved by the GE Contracts Administration, specified performance of the equipment shall be obtained without selection of components whose performance and physical characteristics are unique when compared with vendor stocked or cataloged items and which cannot be ordered by standard nomenclature only.

3.3.1.2.4 Programmable Devices - A firmware document shall be prepared for each unit design requiring firmware. Programmable devices shall be clearly marked and identified.

3.3.1.3 Surface Treatment - All aluminum surfaces shall be chemical-film-treated (iridited) per MIL-C-5541 (Class 3), or MIL-P-53030 Primer before painting. All front panel to cabinet mating surfaces shall be free of paint. Stainless-steel surfaces shall be passivated per MIL-S-5002. Class 1 iridite is permissible when undergoing touch up work.

3.3.1.4 Paint - Panel front and edges, and surfaces exposed when the unit is mounted, shall be painted semigloss gray, Color Chip 26440, per FED-STD-595, with a low volatile organic compound (VOC) polyurethane finish (Cardinal 6400 series). Panel lettering shall be semigloss black chip number 27038.

3.3.1.5 Electrical Grounding and Bonding - Bonding and grounding shall be in accordance with GSFC STDN 270.7. MIL-HDBK-419 shall be used as a reference document. The unit shall have a ground lug located on the rear of the chassis. The lug size shall be either 8/32 or 10/32. The lug (E101) shall provide a ground for the unit.

3.3.1.6 Electrostatic Discharge Protection - Units containing Electrostatic Discharge Sensitive (ESD) devices shall be marked with ESD sensitive device caution labels.

3.3.1.7 Electrical Design

3.3.1.7.1 Electrical Connections

3.3.1.7.1.1 Attachment of Wires and Leads - The equipment shall conform to MIL-STD-454, Requirement 19.

3.3.1.7.1.2 Solderless Wrap - The attachment of wires by solderless wrapping shall conform to MIL-STD-1130.

3.3.1.7.1.3 Soldered Connections - The attachment of wires and leads shall conform to MIL-STD-454, Requirement 5, except resin flux conforming to type RA of QQ-S-571 may be used for electrical and electronic connections. Electrical interconnections and harnesses shall be in accordance with MIL-STD-454 requirements 69 and 71.

3.3.1.7.2 Electrical/Electronic Parts - Electrical/electronic parts shall be selected in accordance with sound engineering practices and in support of the requirements of paragraph 3.2.3. Unless the specific application dictates otherwise, parts shall be of "best commercial quality."

3.3.1.7.3 Electrical Power - The equipment shall operate from the power specified herein.

3.3.1.7.3.1 Single-Phase Power - The unit shall be designed to operate from a two-wire, plus ground, source of 120 volts. The AC power system neutral shall not be connected to the chassis under any circumstances.

3.3.1.7.3.2 Power Transient Susceptibility - Power system transients of as much as a ±10 percent change from the nominal voltage for a period of up to 10 percent of the nominal line frequency will not deteriorate performance of the system. Power transients of a ±10 percent change from the nominal voltage lasting for two (2) seconds shall not prevent satisfactory operation of the equipment immediately following the transient period. Sudden loss of power or prolonged transients of the above type will not damage the equipment.

3.3.1.7.3.3 Overload Protection

a. Electrical overload protection shall meet MIL-STD-454, Requirement 8.

b. A fuse or an overcurrent trip unit of a circuit breaker shall be connected in series with each ungrounded power conductor as determined by the National Electric Code, NFPA 70, for grounded source power.

3.3.1.7.3.4 Primary Circuit Fuses - There are no primary circuit fuses in this unit.

3.3.1.7.3.5 Circuit Breakers

a. When circuit breakers are used, the restoring or switching device shall be readily accessible to the operator.

b. The circuit breaker shall give a visual indication when the breaker is tripped.

c. Holding the switching device closed on an overload shall not prevent tripping of the breaker.

d. Circuit breakers may be mounted on the rear panel and used as on/off switches.

e. Circuit breakers for DC and single-phase AC applications shall conform MIL-C-39019 or commercial equivalent.

3.3.1.7.4 Printed Wiring - Printed wiring shall meet the requirements of MIL-STD-454, Requirement 17. Conformal coating shall not be applied to the printed-wiring assembles.

3.3.1.7.5 Single or Double-Sided Printed Wiring Boards - Single or double-sided printed wiring boards shall conform to MIL-P-55110.

3.3.1.7.6 Multilayer Printed Wiring Boards - Multilayer printed wiring boards shall conform to MIL-P-55110.

3.3.1.7.7 Preferred Circuits

a. In the interest of standardization of circuits, use of standards parts and, ultimately, the collection of circuit performance reliability data, circuits shall be selected whose performance is based on parameters of the parts which are controlled by specification.

b. Conversely, circuit performance shall not be dependent on uncontrolled parameters.

c. Selected circuits shall be such that the use of parts having an approximately normal distribution for those characteristics which are important to the individual applications results in the required equipment performance.

3.3.1.8 Mechanical Design

3.3.1.8.1 Accessibility - Access to enclosures shall be in accordance with MIL-STD-454, Requirement 36.

3.3.1.8.2 Structural Integrity - The unit shall be designed to withstand stresses associated with the transportation, installation, operation, and maintenance of the unit.

3.3.1.8.3 Captive Hardware - Captive hardware shall be used to secure any panel or module which normally would be opened or removed as part of a normal maintenance action.

3.3.1.9 Thermal Design - Thermal design shall be in accordance with Requirement 52 of MIL-STD-454.

3.3.2 Electromagnetic Interference (EMI)
The unit shall meet the following EMI requirements at the rack level:

a. CE-03, Radio Frequency Power Line Conducted Emissions - FCC Class A Limits. Appropriate power line filtering shall be used to satisfy the conducted emission and susceptibility requirements.

b. CE-07, Conducted Switching Spikes - MIL-STD-461 reduced to 5 percent of the line voltage during steady state operation and 50% at turn on and turn off.

c. CS-01, Audio Frequency Power Lead Conducted Susceptibility (30 Hz - 50 kHz) - MIL-STD-461 reduced to 2.5 volts rms from 30 Hz to 13 KHz, then following a straight line to 1.0 volt rms at 50 kHz.

d. CS-02, Radio Frequency Power Line Conducted Susceptibility (.05 to 50 MHz) - MIL-STD-461 reduced to 0.1 volts rms.

e. CS-06, Conducted Spike Susceptibility - MIL-STD-461 reduced to 100 volts peak at 10 microseconds pulse width.

f. RE-02, Radiated Emissions, Electric Field - FCC Class A limit extended down to 15 KHz from 30 MHz, and extended to 10 GHz from 1 GHz with a reduced limit of 20 dBuv/M (measured at 1 meter) from 2.1 to 2.3 GHz. The RE-02 limits specified are granted an additional 20 dB relief due to anticipated rack attenuation.

g. RS-02, Radiated Susceptibility, Magnetic Induction Field, Spikes and Power Frequencies - MIL-STD-461 except reduce the spike voltage to 100 volts peak and power line current (60 Hz) to 2.0 amps.

h. RS-03, Radiated Susceptibility, Electric Fields - MIL-STD-461 except reduce the R.F. field intensity to 0.5 volt/meter from 14 KHz to 2.6 GHz. The R.F. signal will be amplitude modulated, 50 percent at 400 Hz or 1000 Hz.

3.3.2.1 EMI Development Testing - EMI testing shall include development tests of selected components demonstrating potential problems areas. Development tests or analysis, or both shall be performed to gather and verify the characteristics of the identified potential problem areas. EMI tests shall conform with the methods of MIL-STD-462.

3.3.3 Nameplates and Product Marking

A unit nameplate shall be securely attached to the unit. The identifying nameplates shall be in accordance with requirement 67 of MIL-STD-454. The equipment shall be marked with an identifying number in accordance with MIL-STD-130. Electrical parts shall be labeled with designators where necessary to permit ease of identification and shall be uniform throughout the equipment in accordance with requirement 67 of MIL-STD-454. The CAGE Code shall be used in the identification of the equipment. Commercial equipment shall be identified using vendor's standard practices. Front panel legends shall conform to the criteria of paragraph 5.5 of MIL-STD-1472.

3.3.3.1 Location - The general location for the nameplate shall be not more than 6 in. behind the front panel. The preferred location is on the right side panel as one views the front to the rear of the unit.

3.3.4 Workmanship

Workmanship of equipment specified herein shall conform to requirement 9 of MIL-STD-454.

3.3.5 Interchangeability/Producibility

3.3.5.1 Interchangeability - Mechanical and electrical interchangeability shall exist between like assemblies, subassemblies, and replaceable parts regardless of the manufacturer or supplier. The equipment shall be so designed that:

a. Cards and modules normally replaced as part of a maintenance action shall be plug-in design.

b. Replacement of a faulty card and module shall not require the removal of any other card or module.

c. Items with the same identifying part number shall be physically, electrically, and functionally interchangeable.

d. Physically similar, but functionally different cards and modules shall be physically keyed to prevent inadvertent erroneous installation.

e. No card or module replaced as a normal maintenance action shall require alignment or adjustment in the equipment when the replacement is performed, except for power supplies.

3.3.5.2 Producibility - The design shall incorporate features which allow for cost effective production. In this regard, the design shall:

a. Use common materials and processes.

b. Select designs such that automated processes can be used for fabrication.

c. Use multiple sources of supply wherever possible.

d. Use subcontractor standard fabrication, assembly test, and inspection procedures.

3.3.6 Safety

Equipment design shall conform to MIL-STD-454, Requirement 1.

3.3.6.1 Leakage Current - The AC leakage current shall not exceed 5 milliamps (rms), measured at the units input AC Power Safety Ground.

3.3.6.2 Power Supply Protection - Fault conditions ranging from open circuits to short circuits shall cause no damage to the power supply.

3.3.6.3 Equipment Electrical Power On-Off Switch

a. A switch for disconnecting the unit from all electrical power systems shall be mounted on the equipment front panel and its function shall be clearly labeled.

b. A locking type power on-off switch shall break all power conductors of the power circuit.

3.3.6.3.1 Printed Circuit Assembly Protection - Transient Suppression as well as capacitive decoupling shall be provided on all printed circuit assemblies.

3.3.6.4 Power Indicator - A power indicator shall be connected to the load side of the power switch, across the input power conductors, to indicate that the unit is energized.

3.3.6.5 Electrical Cable Protection - Equipment design shall preclude damage to electrical cabling during all normal conditions of assembly, removal, and insertion of equipment when performed by skilled maintenance personnel.

3.3.6.6 Support Strength

a. Slides, detents, mounting surfaces and other attachment mechanisms which support equipment shall have a safety factor equal to twice the maximum anticipated load.

b. Drawer slide design shall include provisions to prevent accidental derailing and detachment of equipment from the shelter.

3.3.6.7 Equipment Access

a. Hinged covers, and sides shall have automatic latch/quick release devices which must be actuated before they can be opened.

b. Sufficient clearance shall be provided in each maintenance configuration to allow tasks to be performed without undue physical discomfort, danger, or effort.

3.3.6.8 Critical Controls - Critical controls, the accidental activation of which may cause damage to equipment, injury to personnel or degradation of system function, shall be designed and located so that they are not susceptible of being accidentally activated.

3.3.6.9 Human Error Design Protection - Operator panel control functions shall be designed in such a manner that neither incorrect adjustment nor random sequencing of functions will cause damage to the equipment.

3.3.6.10 Unacceptable Materials - Equipment design shall not include polychlorinated biphenyls (PCBs), asbestos and asbestos compounds, fragile or brittle materials, beryllium and beryllium compounds unless so identified, and lithium and lithium compounds not specifically approved by the procuring agency.

3.3.6.11 Test Circuit Protection - The maintenance panel and front panel test interfaces shall be suitably protected to prevent equipment damage or personnel hazard during maintenance operations.

3.3.7 Human Performance/Human Engineering
Human engineering design criteria and principles shall be applied in equipment design so as to achieve safe, reliable, and effective performance by the operator and maintenance and control personnel. The guidelines of MIL-STD-1472 shall be used as the criteria for human engineering design.

3.4 Documentation
The plan for prime item documentation is provided in CC Document No. C901E3331, Configuration Management Plan and Procedures for the Second TDRSS Ground Terminal, also known as IEC CM-01/02.

3.5 Logistics
The unit and its major items shall be designed to include provisions for maintenance in compliance with the reliability, maintainability, and interchangeability requirements of 3.2.3, 3.2.4, 3.3.5 and the concepts and criteria described in the following paragraphs.

3.5.1 Maintenance

3.5.1.1 Adjustments - There shall be no maintenance adjustments on this unit except for power supply voltage level settings.

3.5.1.2 Special Support Equipment - During fault isolation, the Performance Measuring and Monitoring Equipment (PMME) and/or the Maintenance Test Group (MTG) may be required.

3.5.1.3 First Level Maintenance - First level maintenance shall consist of fault detection, fault isolation, including isolation capabilities available with built-in-test on line analysis, front panel control, and MTG indicators/test points, followed by removal and replacement of the failed item, reassembly and verification to assure that the system has been restored to operational status. Items replaced during first level maintenance shall be consistent with the line replaceable unit (LRU) concept defined in 3.2.4.1.1.

3.5.1.3.1 Fault Isolation Performance Requirements - The mean time to isolate to an LRU, replacement, and repair inclusive of verification is 25 minutes. The average time to remove and replace an LRU shall not exceed 10 minutes.

3.5.1.3.2 In Circuit Preventive Maintenance - Preventive maintenance shall be capable of being performed on-line without impeding the operational usage of the unit. Preventive maintenance shall take place with the unit in-place and shall not restrict the usage of the unit for periods greater than 1 hour per month.

3.5.1.4 Off-Line Maintenance, Second Level Maintenance - Second level maintenance shall include all repair of failed units or preventive maintenance which is not to be performed in-circuit. Second level maintenance of defective LRU's is normally performed by the vendor's depot facility.

3.6 Personnel and Training
Refer to CCD # C903F3379.

3.7 Major Component Characteristics
The functional, performance and physical requirements and characteristics of each major component of this unit are given in the performance specifications referenced in IEC drawing number 7472502.

3.8 Precedence
The order of precedence with respect to the requirements specified in this document is:

(1) This specification, 7472506;

(2) The General Electric specifications as traced in the Traceability Matrix of Appendix III of this document.

(3) SOW-GE-STGT-8701, Statement of Work (SOW) for USS SSA Equipment HWCI, KSAR Low Data Rate Equipment HWCI, MA RCVR/XMTR Equipment HWCI. Revision 5, 28 November 1989.

4.0 QUALITY ASSURANCE PROVISIONS

4.1 General

This section defines the requirements for verification of performance and design characteristics specified in Section 3 of this specification. The subcontractor is required to implement and maintain a Quality Assurance (QA) Program in accordance with the SOW. In the event of conflict between this specification and the SOW, the SOW takes precedence. This program applies to all work accomplished by the subcontractors and suppliers, including subtier sources and other divisions or subsidiaries of the subcontractor (hereafter termed subcontractor) who provide parts, materials, components, systems, and software as described in the contract Statement of Work.

The subcontract shall verify that his procurement documents impose the applicable section of this document on his subcontractors and other suppliers. These subcontractors and other suppliers shall, in turn impose these standards on their procurement sources.

Verification will include:

a. Inspection (in-coming, in-process and final)
b. Tests
c. Demonstration
d. Analysis

4.1.1 Responsibility for Verifications

Unless otherwise specified in the contract or order, the subcontractor is responsible for the performance of all verification requirements as specified herein. Except as otherwise specified, the subcontractor may utilize his own facilities or any commercial laboratory acceptable to GE. GE reserves the right to perform any of the verifications set forth in the specification where such verifications are deemed necessary to assure supplies and services conform to prescribed requirements.

4.1.1.1 Quality Assurance Requirement - Quality assurance requirements shall be in conformance with the Statement of Work (SOW).

4.2 Quality Conformance Verifications

Appendix IV defines the method of verification (test, inspection, demonstration, analysis) for each requirement specified in Section 3. All testing shall be performed using calibrated test instrumentation. All data taken during the verification test shall be validated by the subcontractor QA personnel and made available to the GE and NASA QA representative.

4.2.1 Test

Tests identified in Appendix IV shall be performed to verify that the hardware conforms to the operational parameters as defined in the applicable paragraph of Section 3. All verification testing shall be performed at ambient conditions. No environmental tests are required.

4.2.2 Inspections

Inspections shall be in accordance with subcontractor's STGT Quality Assurance Plan. Inspections are visual investigations of design, production, or test documentation, or the observation/measurement of hardware/software characteristics to determine compliance with specified requirements. Requirements of Section 3 that are satisfied by inspection are identified in Appendix IV.

4.2.3 Demonstration

Demonstrations are the exercise of hardware/software operations to assure that special qualitative functions and capabilities can be performed in accordance with applicable specifications.

4.2.4 Analysis

Where applicable, the verification of some technical parameters and performance will be accomplished by analysis. Analysis is the mathematical treatment including computer analysis of appropriate models to determine compliance with specified requirements where test, demonstration and inspection are not feasible. Analysis may be performed with as-built test results or as-built data to provide formal verification of a requirement. Analysis shall be documented in SDRL Supporting Engineering Analysis and Data (HE-08).

4.2.5 Method Annotation

An X is placed in the applicable column of Appendix IV to mark the verification method for each requirement.

Where an X(P) is placed in one column of Appendix IV and an X(S) is placed in one or more of the other columns, this means that the method marked X(P) is the primary verification method, but it must use supporting data gathered from the results of the other methods. An X is placed in the N/A column for Non-Applicable or Non-Requirements such as summary or introductory paragraphs.

5.0 PREPARATION FOR DELIVERY

Preparation for delivery shall be in accordance with NHB-6000.1C. No non-standard practices are required.

6.0 NOTES

No additional notes or instructions are required.

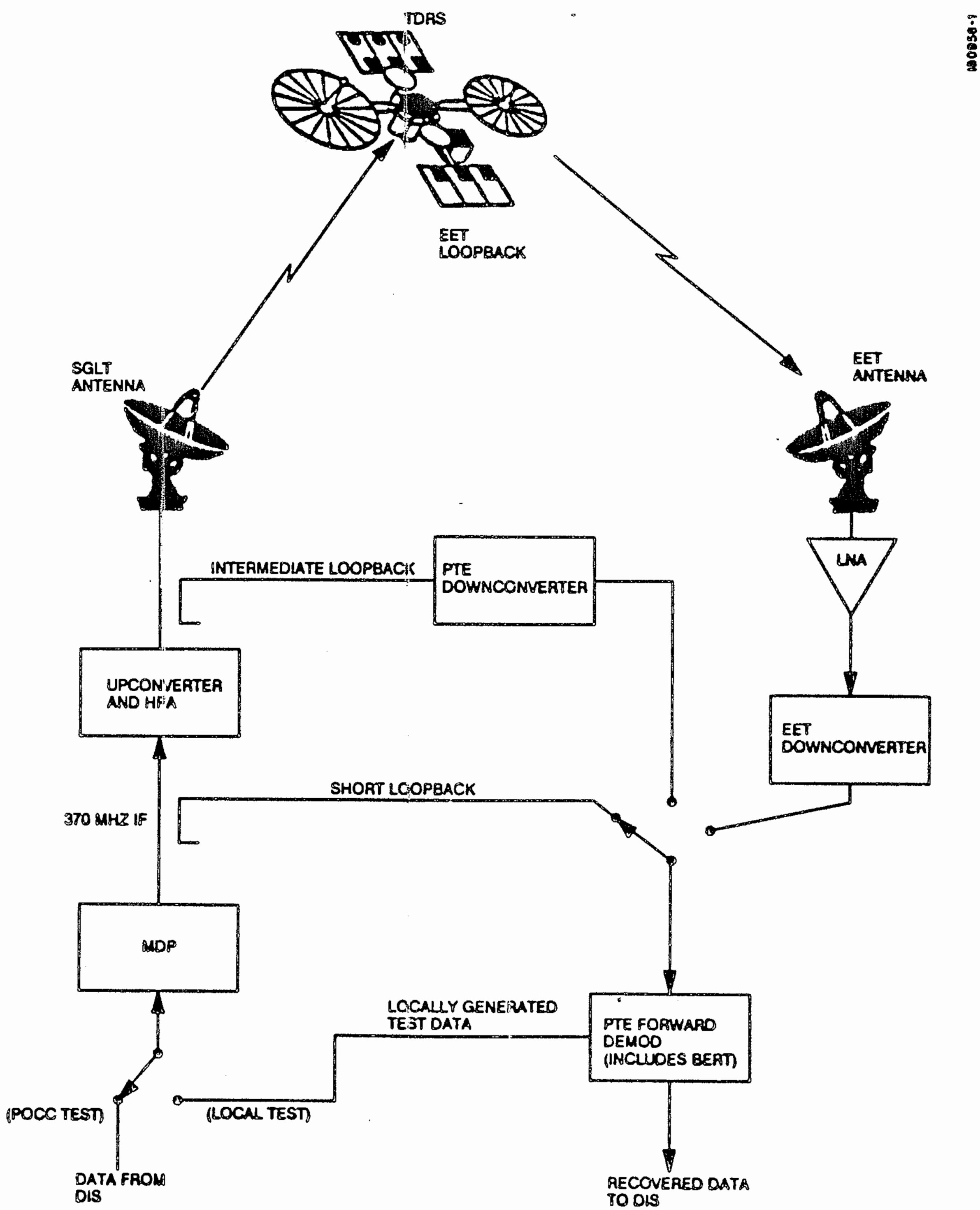


Figure 1. Forward Loop Tests for SSA

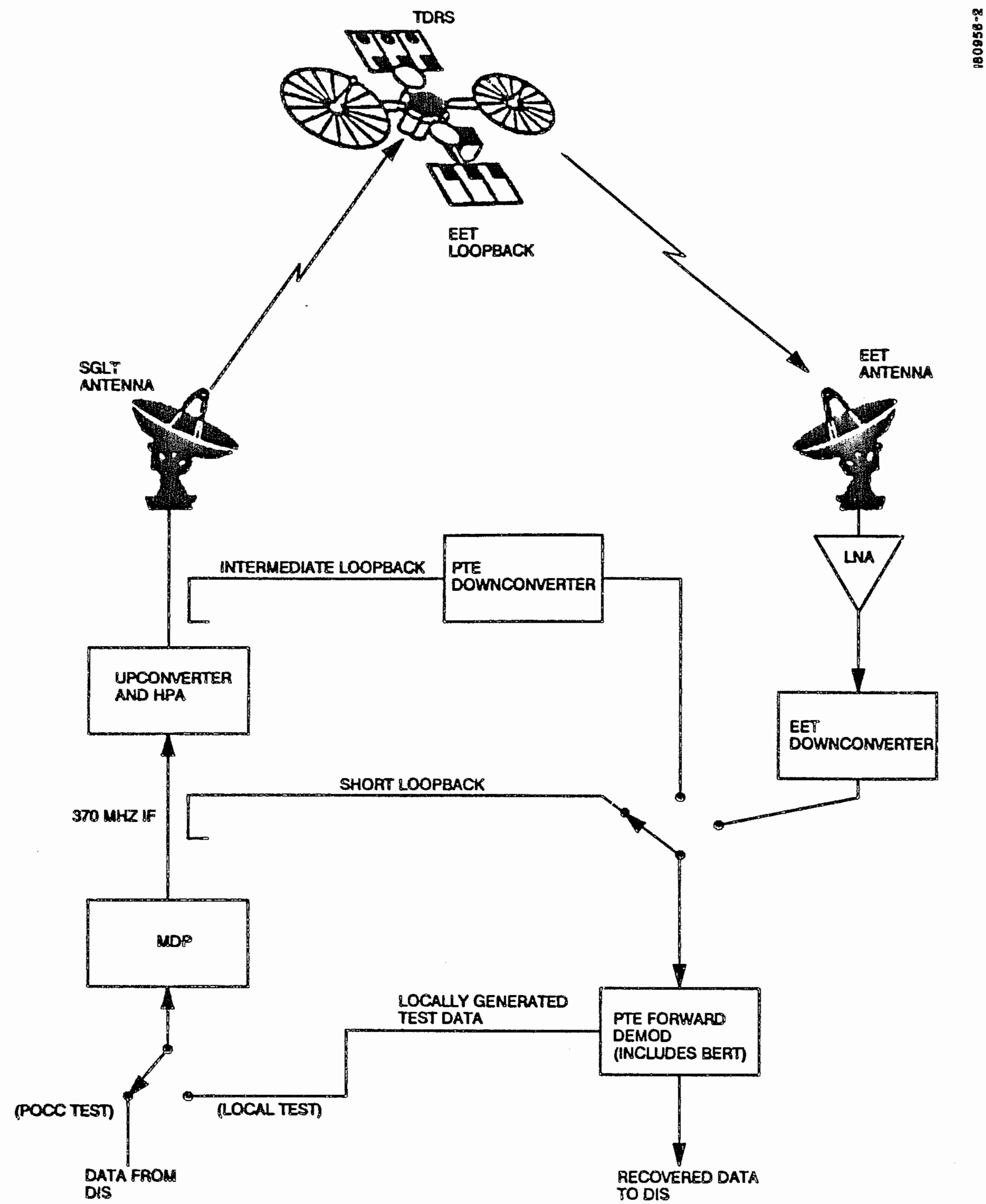


Figure 2. Forward Loop Tests for KSA

INTERSTATE ELECTRONICS CORPORATION A Figgie International Company	SHEET NUMBER	DOCUMENT NUMBER	REV
	F-2	7472506	C

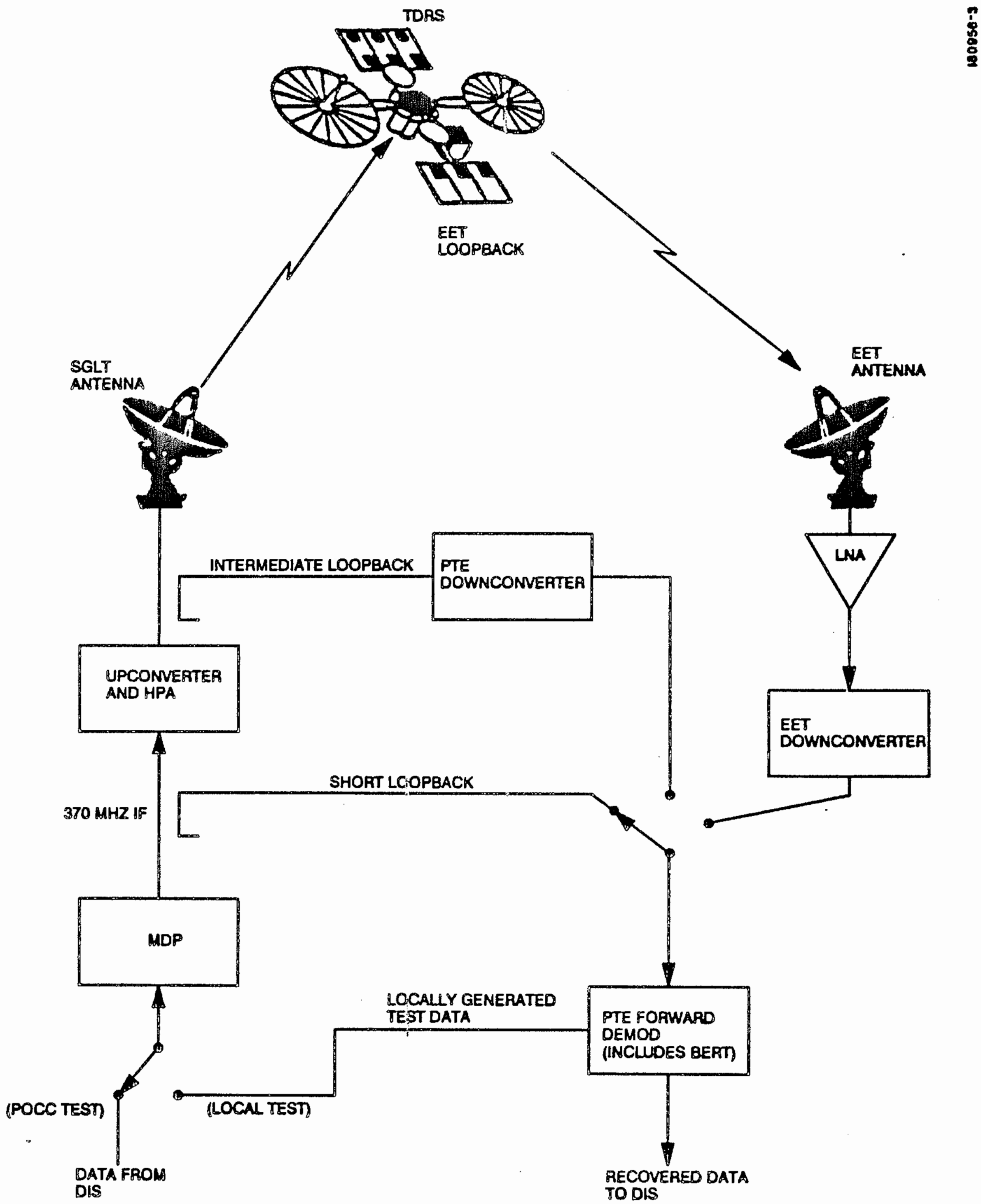


Figure 3. Forward Loop Tests for MA

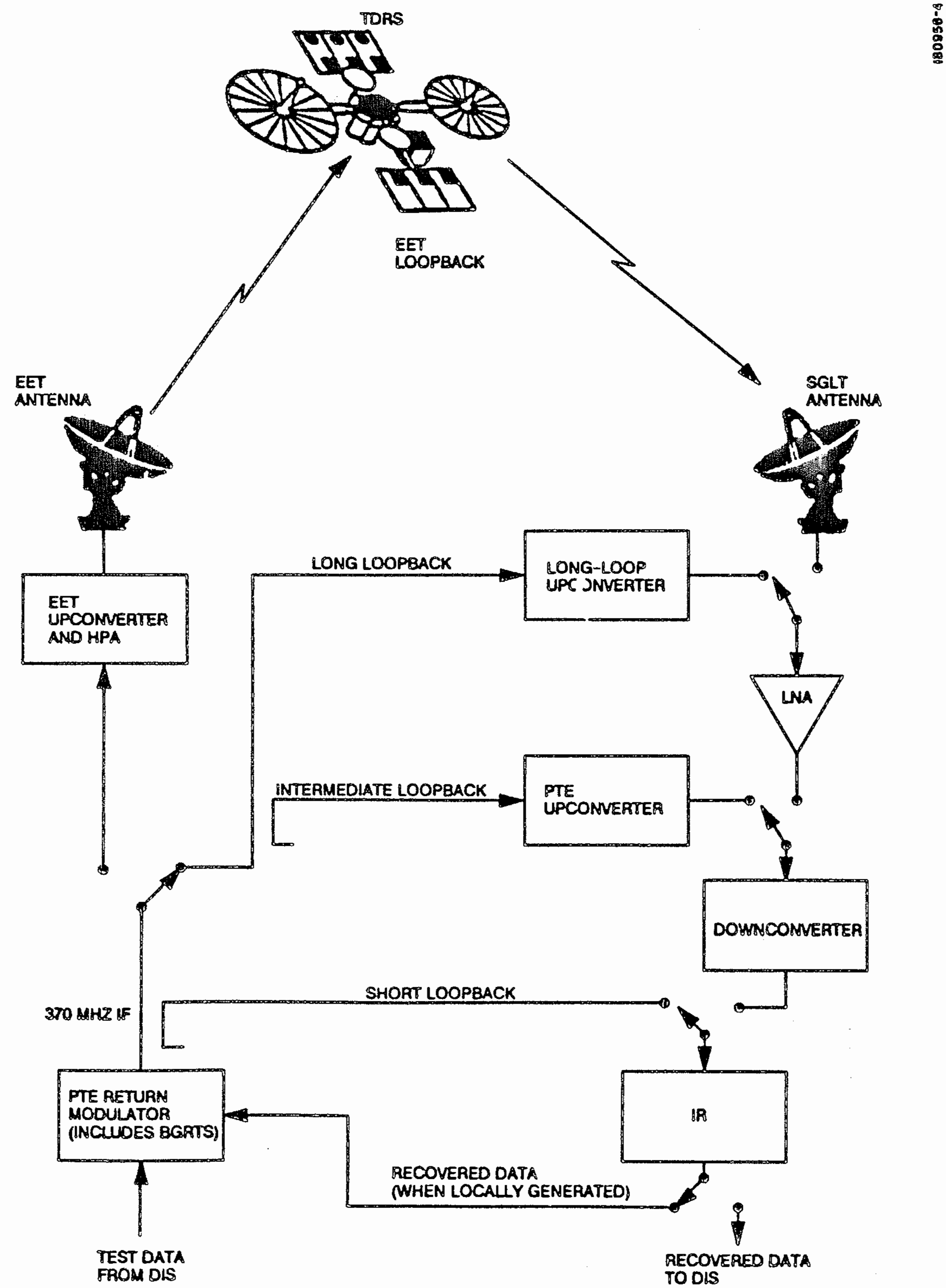


Figure 4. Return Loop Tests for SSA

INTERSTATE ELECTRONICS CORPORATION A Figgie International Company	SHEET NUMBER	DOCUMENT NUMBER	REV
	F-4	7472506	C

IEC R-508-1 (REV.10/83)

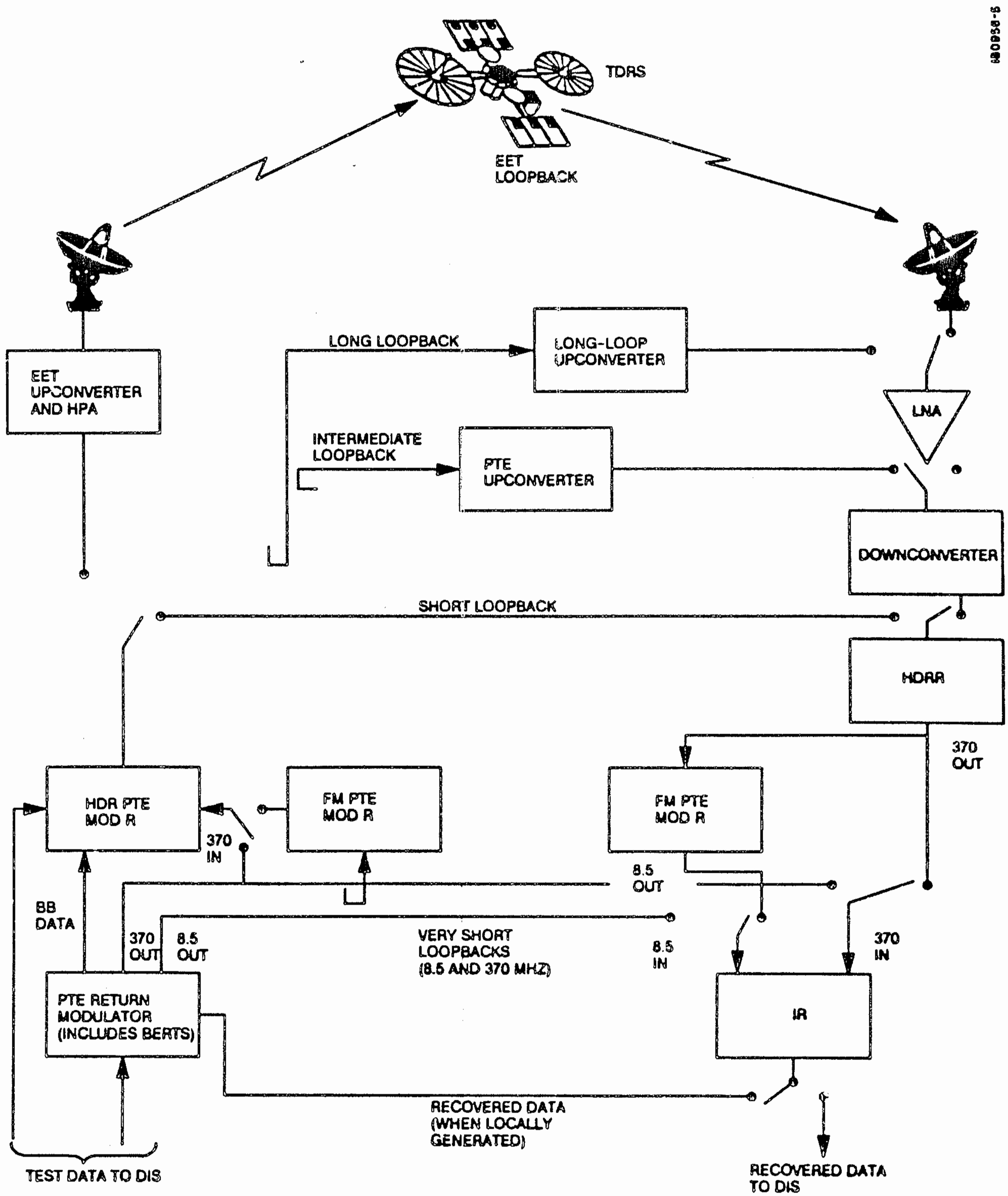


Figure 5. Return Loop Tests for KSA

INTERSTATE ELECTRONICS CORPORATION A Figgie International Company	SHEET NUMBER	DOCUMENT NUMBER	REV
	F-5	7472506	C

IEC R-508-1 (REV.10/83)

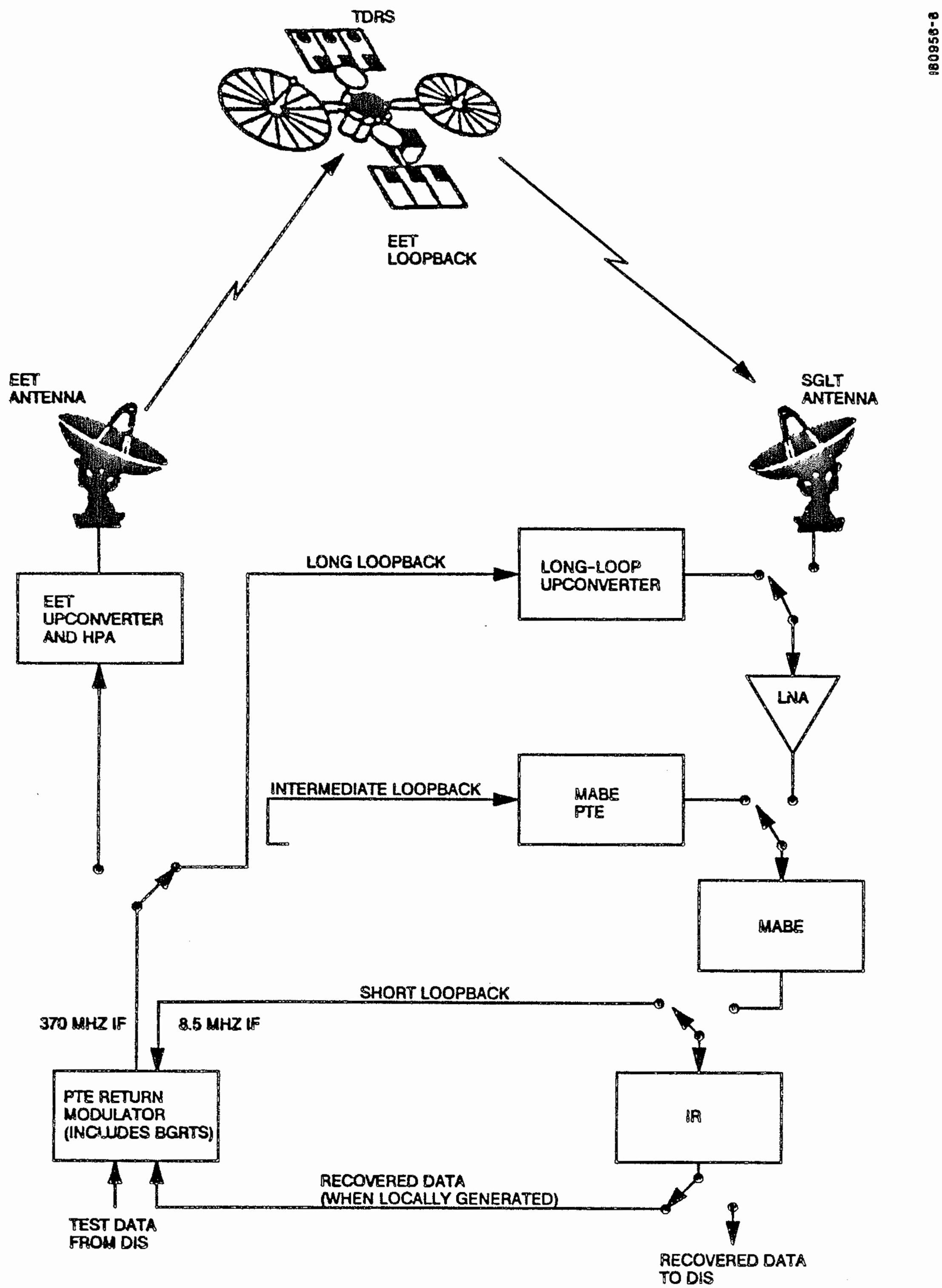


Figure 6. Return Loop Tests for MA

180956-7

Figure 7. Test Modem Interfaces

Figure 8. Test Modem Block Diagram

INTERSTATE ELECTRONICS CORPORATION A Figgie International Company	SHEET NUMBER F-8	DOCUMENT NUMBER 7472506	REV C

IEC R-508-1 (REV.10/83)

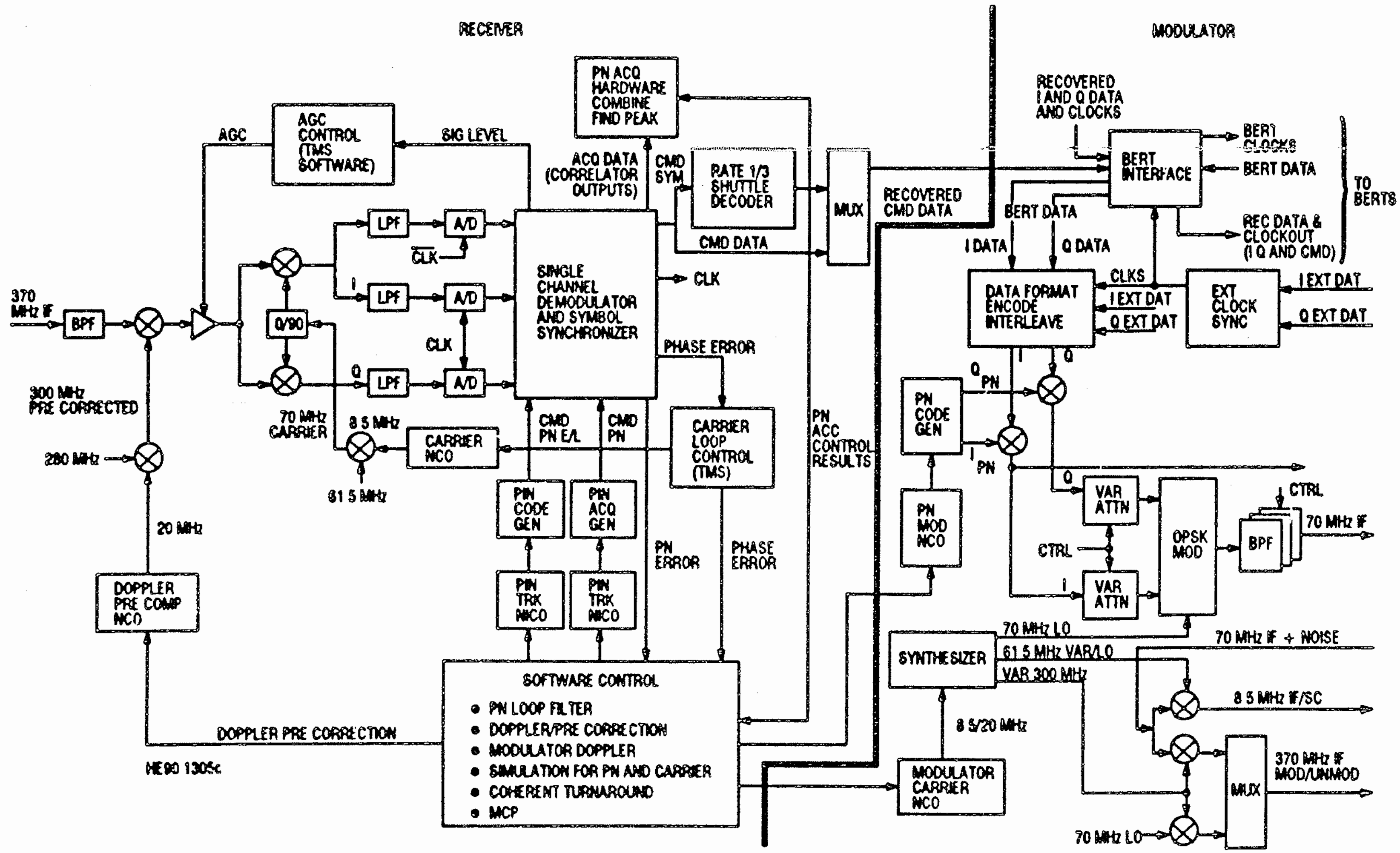


Figure 9. Test Modem Functional Flow

INTERSTATE ELECTRONICS CORPORATION A Figgie International Company	SHEET NUMBER	DOCUMENT NUMBER	REV
	F-9	7472506	C

IEC R-508-1 (REV. 10/83)

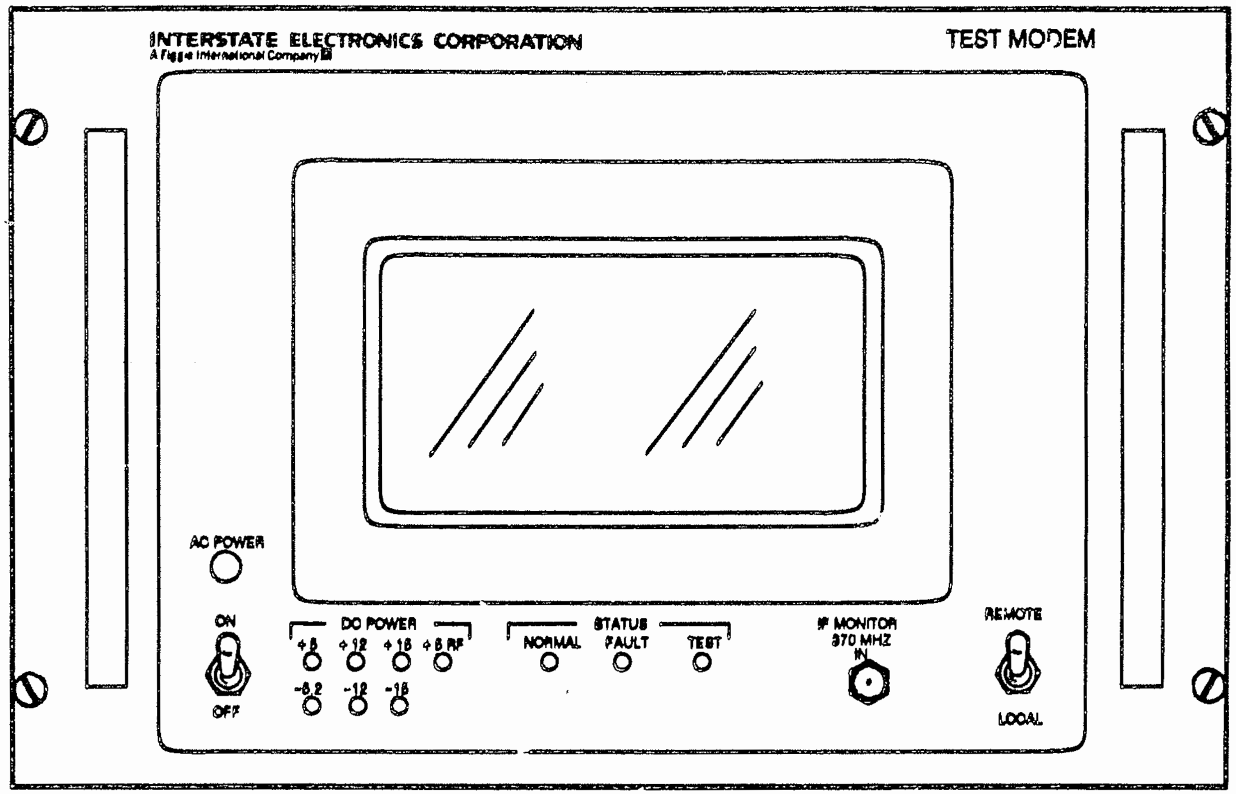


Figure 10. Test Modem Front Panel

180958-9

INTERSTATE ELECTRONICS CORPORATION A Figgie International Company	SHEET NUMBER F-10	DOCUMENT NUMBER 7472506	REV C

IEC R-508-1 (REV.10/83)

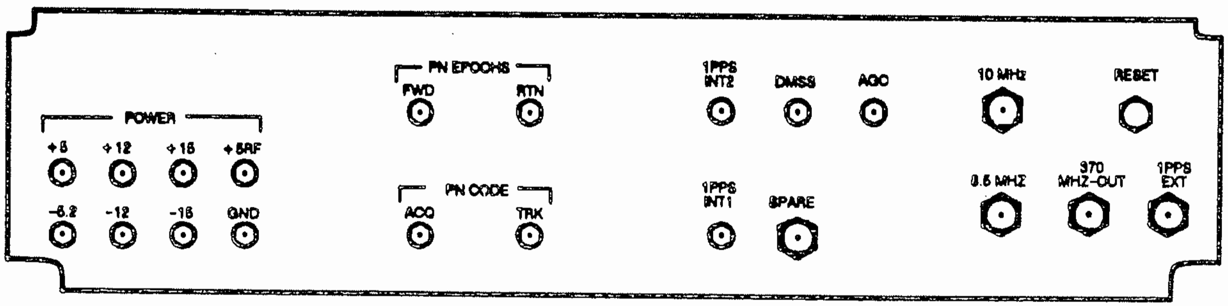
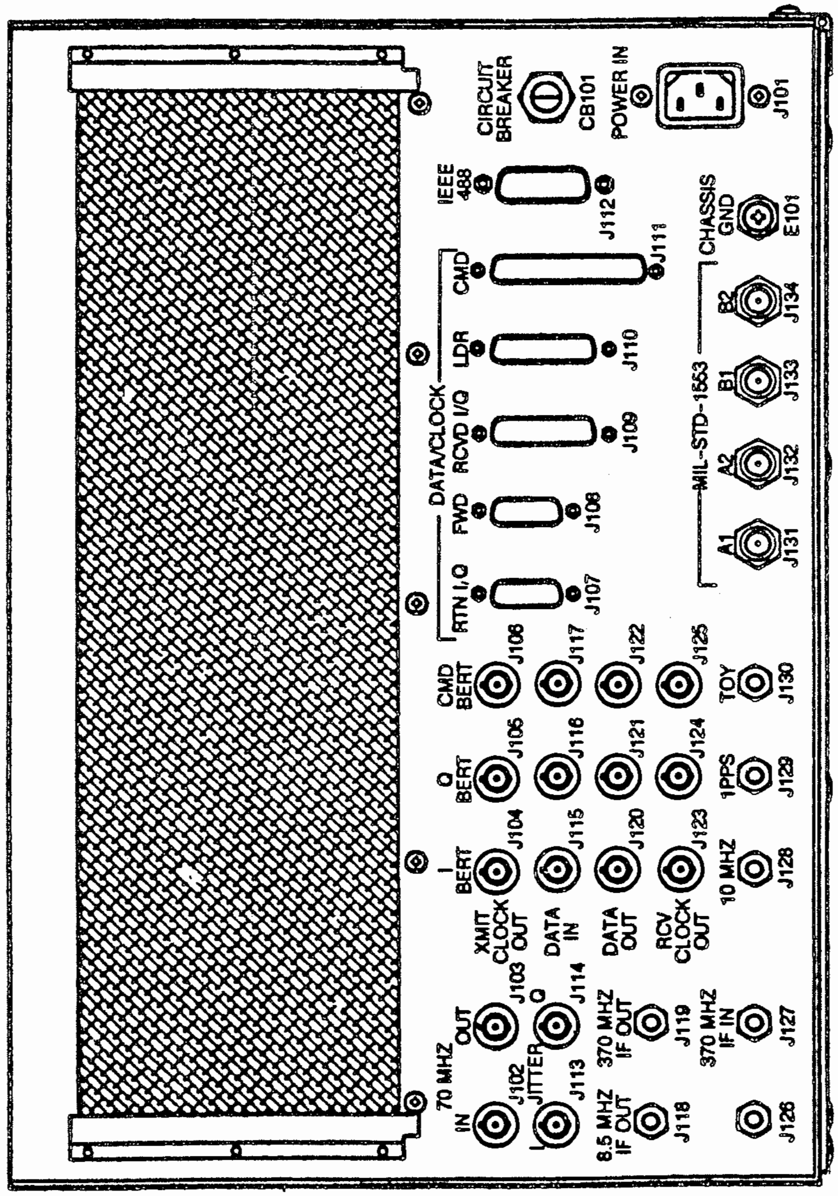


Figure 11. Test Modem Maintenance Panel

180956-10

INTERSTATE ELECTRONICS CORPORATION A Figgie International Company	SHEET NUMBER	DOCUMENT NUMBER	REV
	F-11	7472506	C

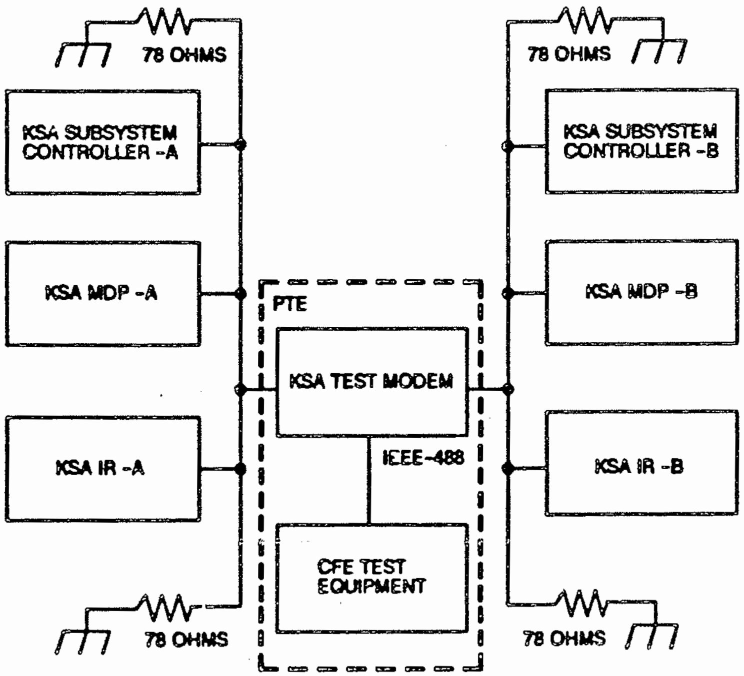
IEC R-508-1 (REV.10/83)



380956-11

Figure 12. Test Modem Back Panel

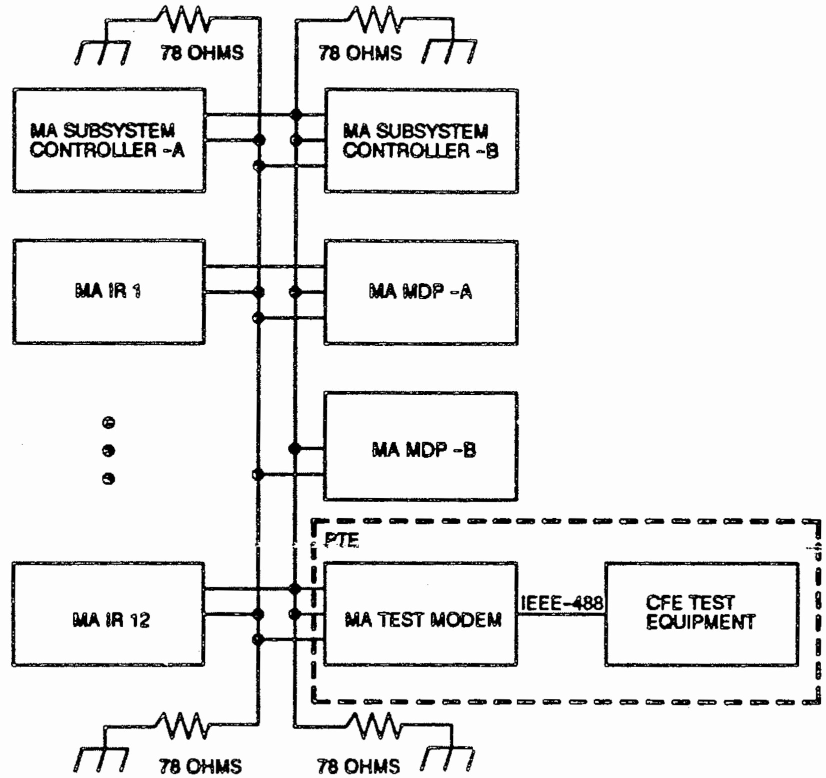
INTERSTATE ELECTRONICS CORPORATION A Figgie International Company	SHEET NUMBER	DOCUMENT NUMBER	REV
	F-12	7472506	C



NOTE:

1. EACH 1553B BUS PORT IS TRANSFORMED COUPLED.
2. BOTH CONTROLLERS SIMULATANEOUSLY INTERFACE TO THEIR OWN IR/MDP's AND SHARE A PTE.
3. TEST MODEM RESPONDS TO COMMANDS FROM BOTH SUBSYSTEM CONTROLLERS, AND STATUS IS AVAILABLE TO BOTH SUBSYSTEM CONTROLLERS.

KSA & SSA
CONFIGURATION



NOTE:

1. EACH 1553B BUS PORT IS TRANSFORMED COUPLED.
2. BOTH CONTROLLERS INTERFACE WITH MA EQUIPMENT, BUT ONLY ONE CONTROLLER IS ACTIVE AT A TIME.

MA
CONFIGURATION

Figure 13. MIL-STD-1553B Data Bus Implementation

80956-12

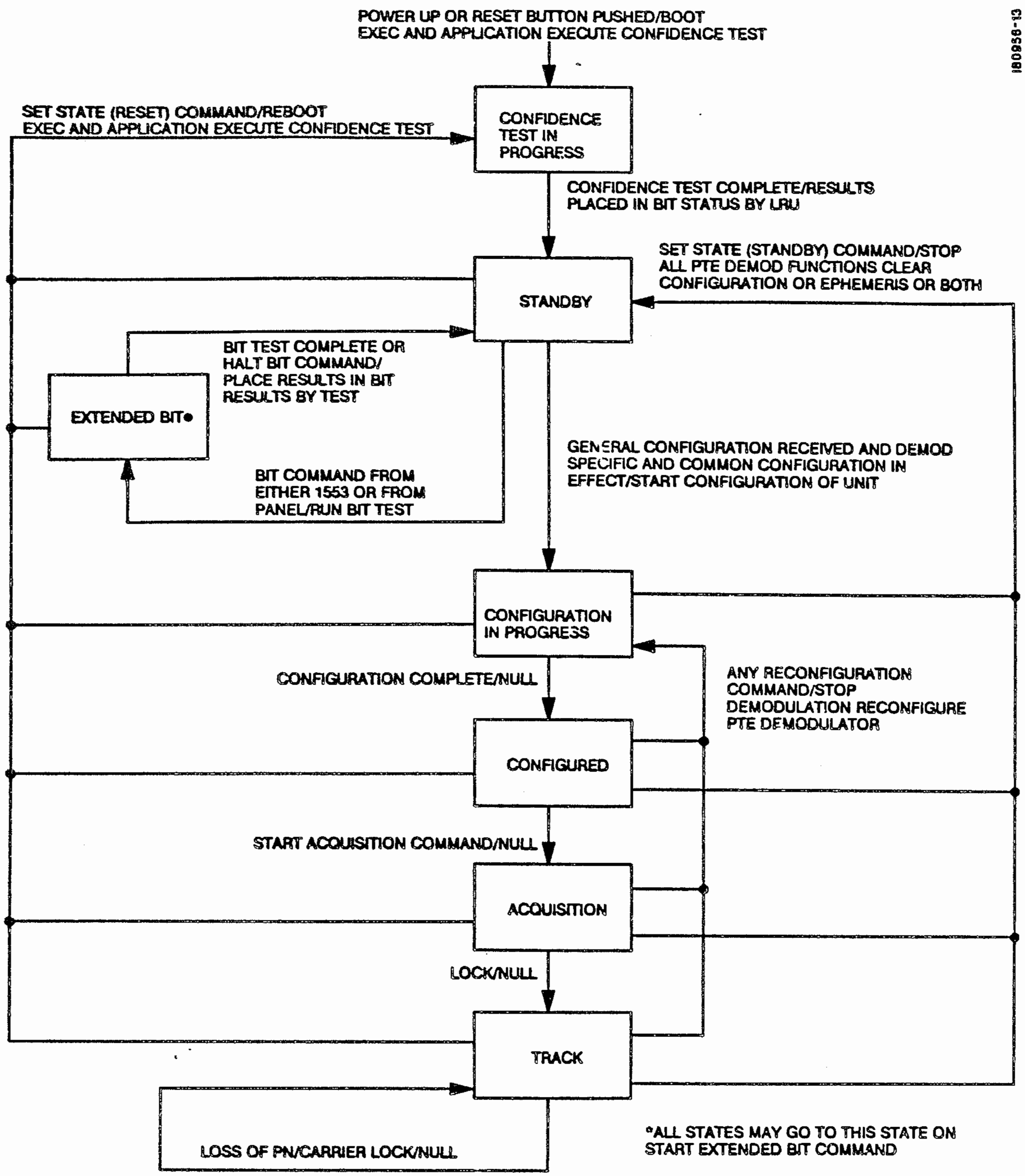


Figure 14. State Transition Diagram for Forward Demodulator Noncoherent Turnaround

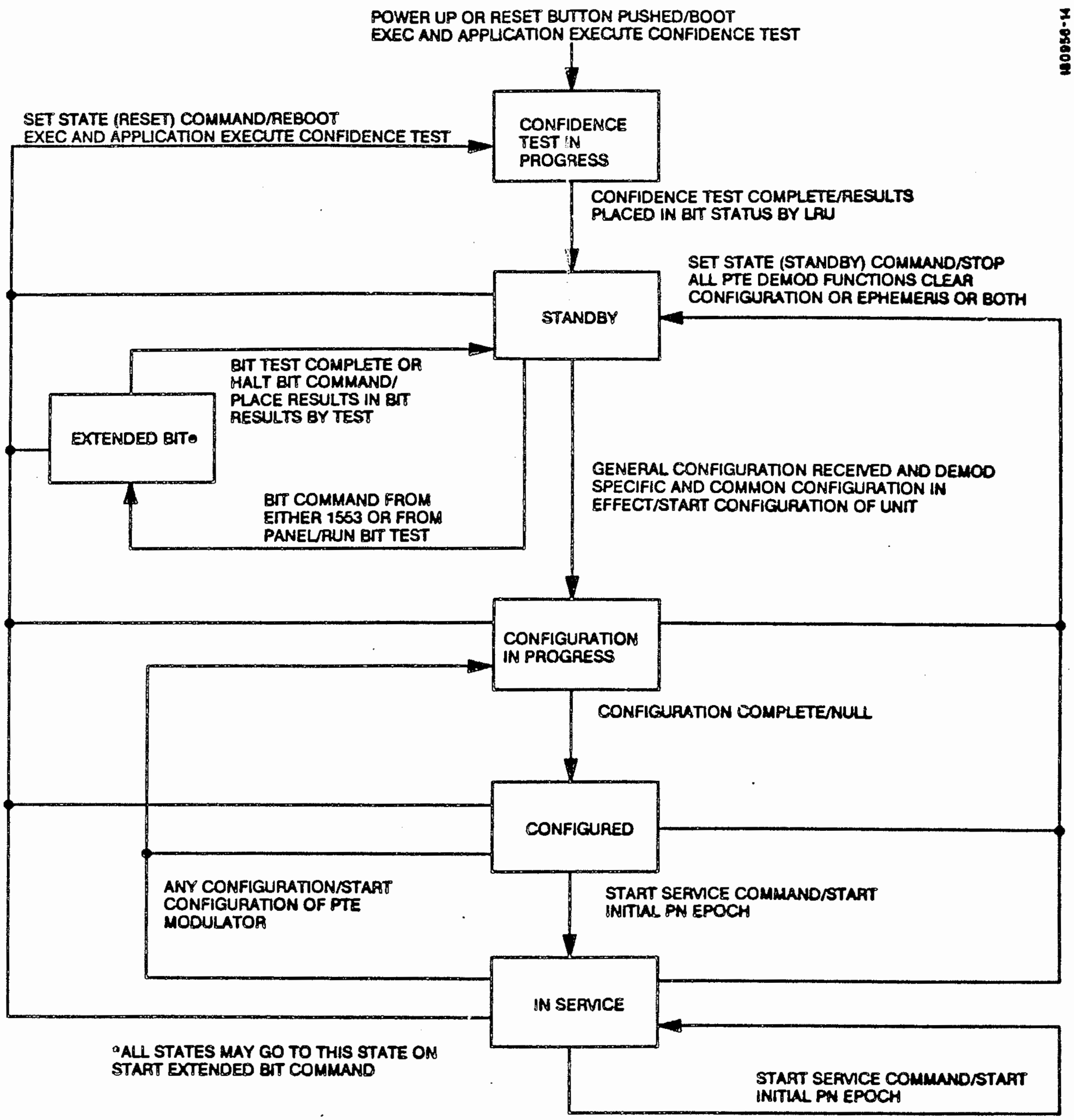


Figure 15. State Transition Diagram for Return Modulator Noncoherent Turnaround

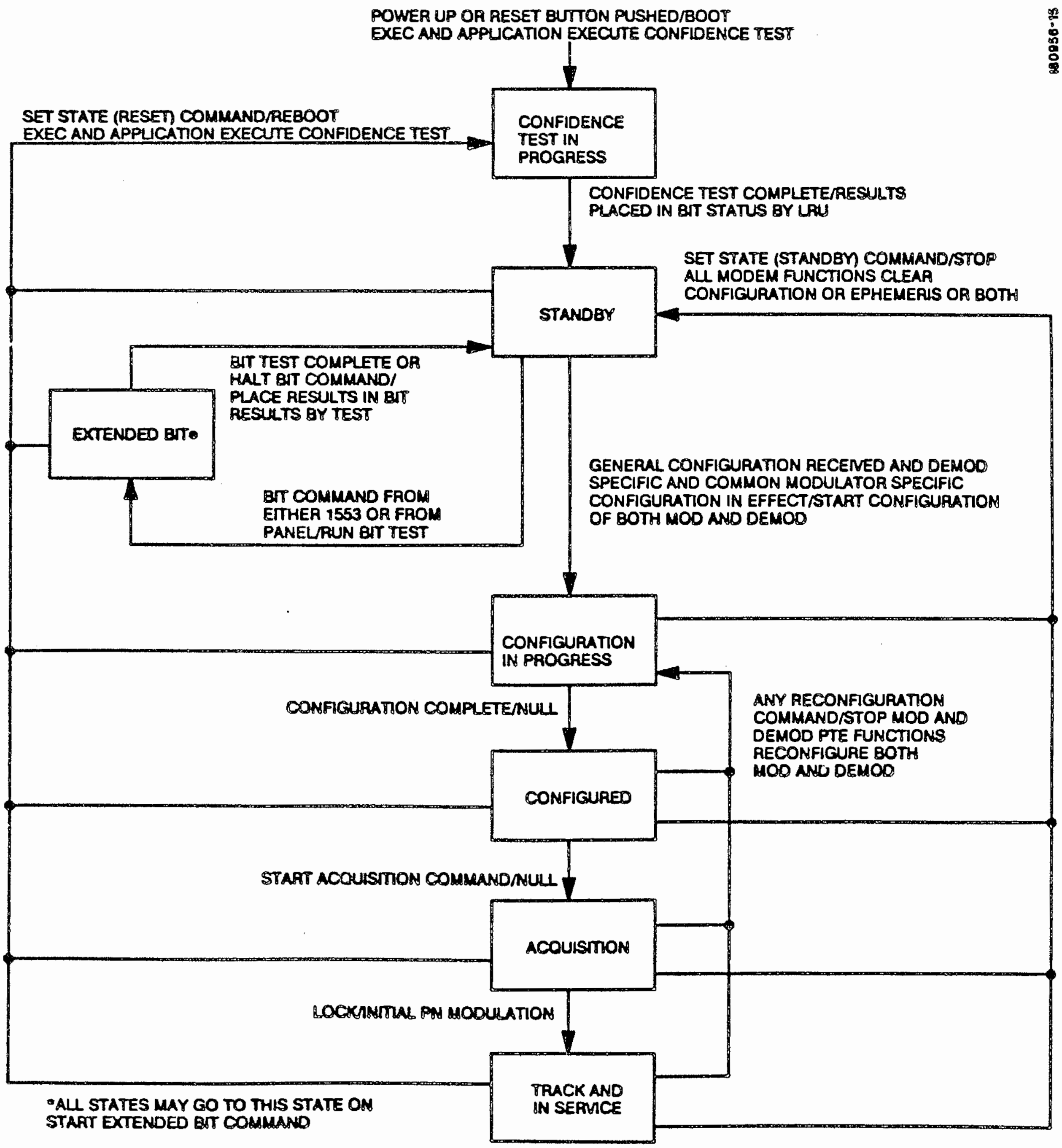


Figure 16. State Transition Diagram for Test Modem Coherent Turnaround

80958-98

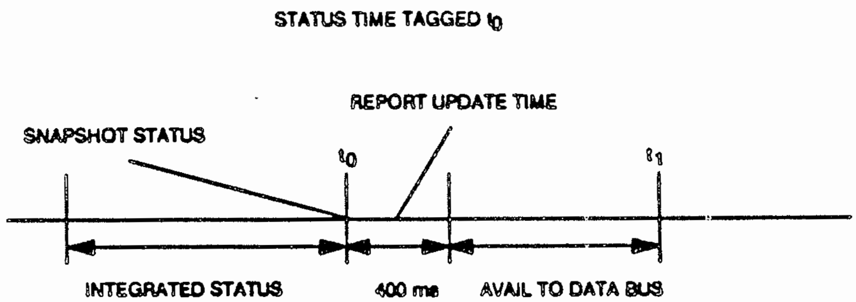


Figure 17. Timing Report Collection

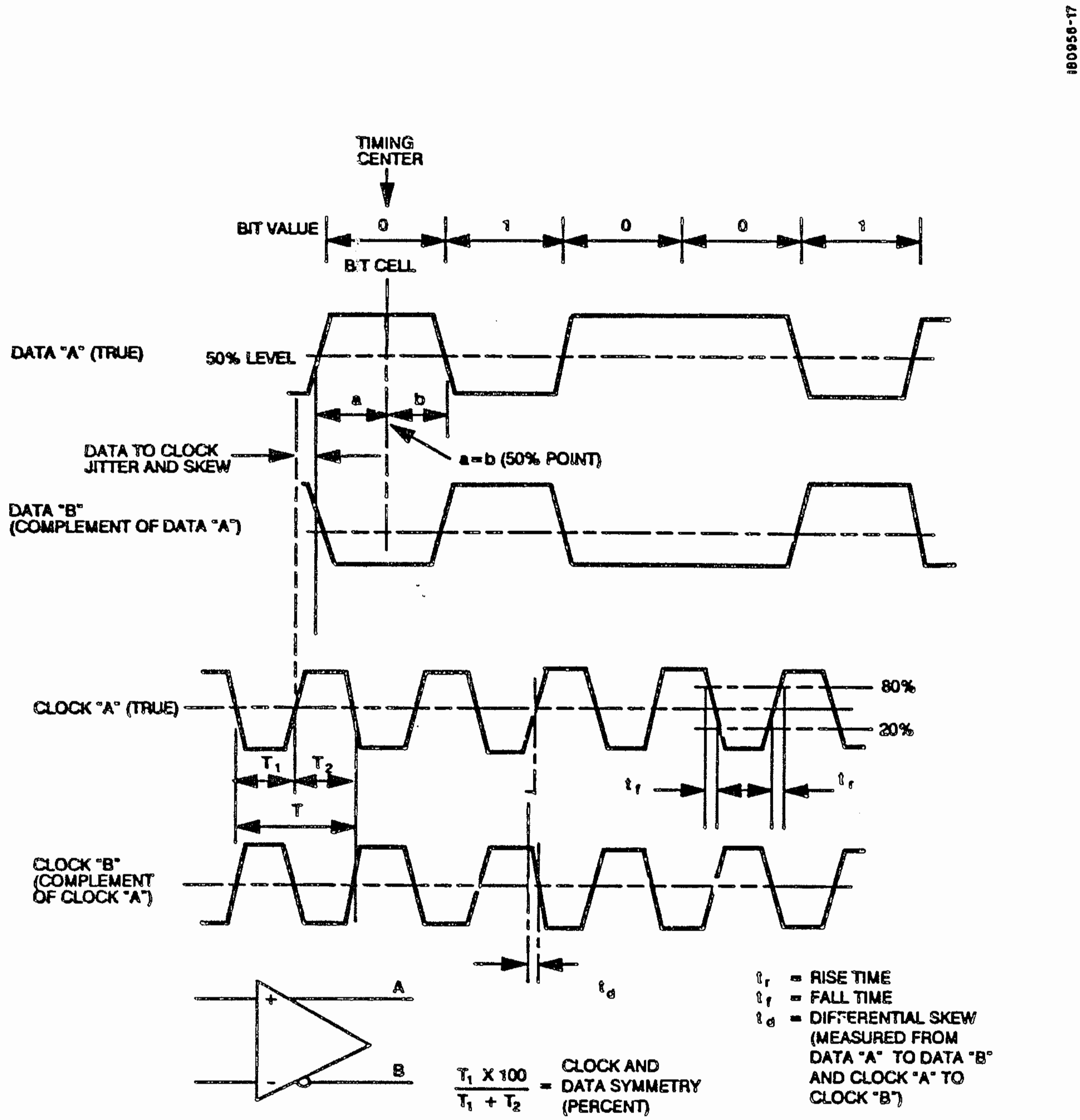


Figure 18. Clock and Data Relationships

TABLE I. PRIMARY INTERFACE BACK PANEL CONNECTORS AND SIGNALS

Signal Identification and Connector Termination of Back Panel Signals for the Primary Interface of the Test Modem

Signal Name	Unit Connector Terminal Number and Type		
Primary AC Power	J101	Input	AC Connector
115 VAC Return (white)	J101-A		
Safety Ground (green)	J101-B		
115 VAC Line (black)	J101-C		
I and Q Simulated User Return Data and Clock Inputs	J107	Inputs	15 pin male D type
External I Data +			
External I Data -	J107-01		
Shield Ground	J107-02		
	J107-09		
External I Clock +			
External I Clock -	J107-03		
Shield Ground	J107-04		
	J107-10		
External Q Data +			
External Q Data -	J107-05		
Shield Ground	J107-06		
	J107-14		
External Q Clock +			
External Q Clock -	J107-07		
Shield Ground	J107-08		
	J107-15		
PTE Baseband Command Data/Clock Outputs	J108	Outputs	15 pin female D type
Cmd Chan Recovered Data +	J108-01		
Cmd Chan Recovered Data -	J108-02		
Shield Ground	J108-09		
Cmd Chan Recovered Clock +	J108-03		
Cmd Chan Recovered Clock -	J108-04		
Shield Ground	J108-10		

Table I. (continued)

Signal Identification and Connector Termination of Back Panel Signals for the Primary Interface of the Test Modem			
Signal Name	Unit Connector Terminal Number and Type		
PTE Baseband Data/Clock Inputs	J109	Inputs	25 pin male D
A Side Remote Terminal Address			type
Remote Terminal Address 0			
Remote Terminal Address 1			
Remote Terminal Address 2	J109-01		
Remote Terminal Address 3	J109-02		
Remote Terminal Address 4	J109-03		
Remote Terminal Parity	J109-04		
Remote Terminal Return	J109-05		
	J109-06		
Recovered I Data +	J109-07		
Recovered I Data -			
Shield Ground	J109-08		
	J109-09		
Recovered I Clock +	J109-23		
Recovered I Clock -			
Shield Ground	J109-10		
	J109-11		
Recovered Q Data +	J109-24		
Recovered Q Data -			
Shield Ground	J109-12		
	J109-13		
Recovered Q Clock +	J109-25		
Recovered Q Clock -			
Shield Ground	J109-14		
	J109-15		
	J109-16		

Table I. (continued)

Signal Identification and Connector Termination of Back Panel Signals for the Primary Interface of the Test Modem			
Signal Name	Unit Connector Terminal Number and Type		
PTE Low Data Rate Baseband Data Outputs	J110	Outputs	25 pin female D type
Low Data Rate Data +	J110-01		
Low Data Rate Data -	J110-02		
Shield Ground	J110-09		
Low Data Rate Clock +	J110-03		
Low Data Rate Clock -	J110-04		
Shield Ground	J110-10		
Recovered Forward Data and Clock Outputs	J111		37 pin female D type
B Side Remote Terminal Address			
Remote Terminal Address 0			
Remote Terminal Address 1	J111-01	Inputs	
Remote Terminal Address 2	J111-02		
Remote Terminal Address 3	J111-03		
Remote Terminal Address 4	J111-04		
Remote Terminal Parity	J111-05		
Remote Terminal Return	J111-06		
	J111-07		
Command Data TTL +			
Command Data TTL -	J111-08	Outputs	
Shield Ground	J111-09		
	J111-25		
Command Clock TTL +			
Command Clock TTL -	J111-10	Outputs	
Shield Ground	J111-11		
	J111-26		
PTE 8.5 MHz IF Output	J118	Output	SMA FEMALE
PTE 370 MHz IF Output	J119	Output	SMA FEMALE
PTE 370 MHz IF Input	J127	Input	SMA FEMALE
CTFS 10 MHz	J128	Input	SMA FEMALE
CTFS 1 PPS	J129	Input	SMA FEMALE

Table I. (continued)

Signal Identification and Connector Termination of Back Panel Signals for the Primary Interface of the Test Modem			
Signal Name	Unit Connector Terminal Number and Type		
CTFS TOY	J130	Input	SMA FEMALE
MIL-STD-1553B Bus 1A Bus HI (blue) Bus LO (white) Shield	J131 Center Inner Shield	Input/ Output	TWINAX
MIL-STD-1553B Bus 2A Bus HI (blue) Bus LO (white) Shield	J132 Center Inner Shield	Input/ Output	TWINAX
MIL-STD-1553B Bus 1B Bus HI (blue) Bus LO (white) Shield	J133 Center Inner Shield	Input/ Output	TWINAX
MIL-STD-1553B Bus 2B Bus HI (blue) Bus LO (white) Shield	J134 Center Inner Shield	Input/ Output	TWINAX

TABLE II. TEST EQUIPMENT INTERFACE BACK PANEL CONNECTORS AND SIGNALS

Signal Identification and Connector Termination of Back Panel Signals for the Test Equipment Interface of the Test Modem			
Signal Name	Unit Connector Terminal Number and Type		
70 MHz IF Input	J102	Input	BNC FEMALE
70 MHz IF Output	J103	Output	BNC FEMALE
I Channel Transmit Clock	J104	Output	BNC FEMALE
Q Channel Transmit Clock	J105	Ouput	BNC FEMALE
Command Channel Transmit Clock	J106	Output	BNC FEMALE
IEEE-488 Data Bus	J112	Input/ Output	24 pin cinch
DIO1	J112-01		
DIO2	J112-02		
DIO3	J112-03		
DIO4	J112-04		
EOI	J112-05		
DAV	J112-06		
NRFD	J112-07		
NDAC	J112-08		
IFC	J112-09		
SRQ	J112-10		
ATN	J112-11		
SHIELD	J112-12		
DIO5	J112-13		
DIO6	J112-14		
DIO7	J112-15		
DIO8	J112-16		
REN	J112-17		
GND	J112-18		
GND	J112-19		
GND	J112-20		
GND	J112-21		
GND	J112-22		
GND	J112-23		
GND	J112-24		
I Channel Data	J115	Input	BNC FEMALE
Q Channel Data	J116	Input	BNC FEMALE
Command Channel Data	J117	Input	BNC FEMALE
I Channel Received Data	J120	Output	BNC FEMALE
Q Channel Received Data	J121	Output	BNC FEMALE
Command Channel Received Data	J122	Output	BNC FEMALE

Table II. (continued)

Signal Identification and Connector Termination of Back Panel Signals for the Test Equipment Interface of the Test Modem			
Signal Name	Unit Connector Terminal Number and Type		
I Channel Received Clock	J123	Output	BNC FEMALE
Q Channel Received Clock	J124	Output	BNC FEMALE
Command Channel Received Clock	J125	Output	BNC FEMALE

TABLE III. MAINTENANCE PANEL CONNECTORS AND SIGNALS

Signal Identification and Connector Termination of Back Panel Signals for the Maintenance Panel of the Test Modem			
Signal Name	Unit Connector Terminal Number and Type		
+ 5 Volts DC	T1	Output	Phone Jack
+ 12 Volts DC	T2	Output	Phone Jack
+ 15 Volts DC	T3	Output	Phone Jack
+ 5 Volts DC (RF)	T4	Output	Phone Jack
- 5 Volts DC	T5	Output	Phone Jack
- 12 Volts DC	T6	Output	Phone Jack
- 15 Volts DC	T7	Output	Phone Jack
Ground	T8	Output	Phone Jack
Forward PN Epoch	T9	Output	Phone Jack
Return PN Epoch	T10	Output	Phone Jack
DMSS	T11	Output	Phone Jack
Acquisition PN Code	T12	Output	Phone Jack
Tracking PN Code	T13	Output	Phone Jack
1 PPS Internal (2)	T14	Output	Phone Jack
1 PPS Internal (1)	T15	Output	Phone Jack
Automatic Gain Control	T16	Output	Phone Jack
CTFS 10 MHz	J1	Output	BNC Female
370 MHz	J2	Output	BNC Female
Spare	J3	Output	BNC Female
8.5 MHz	J4	Output	BNC Female
CTFS 1 PPS External	J5	Output	BNC Female

TABLE IV. ADDITIONAL TEST POINT CONNECTORS AND SIGNALS

Signal Identification and Connector Termination of Back Panel Signals for Additional Test Points of the Test Modem			
Signal Name	Unit Connector Terminal Number and Type		
IF Monitor 370 MHz In	J1 Front Panel	Output	
I Jitter	J113 Back Panel	Input	BNC FEMALE
Q Jitter	J114 Back Panel	Input	BNC FEMALE
Spare	J126 Back Panel	Spare	BNC FEMALE

TABLE V. IDENTIFICATION OF CONNECTOR TYPES

Connector Type	IEC Part Number	Vendor Part Number
AC Connector	338-020-090	LE10BC
SMA Female Connector	374-215-001	2084-0000-00
BNC Female Connector	374-019-017	3284-2240-00
Twinax (Threaded)	374-150-023	BJ379-47
15 Pin Male Type D	373-043-989	17-22015-1(439)
15 Pin Female Type D	373-049-002	M24308/2-7
24 Pin Cinch	373-048-020	57-20240-2
25 Pin Male Type D	373-043-990	17-22025-1(439)
25 Pine Female Type D	373-049-003	M24308/2-8
37 Pin Female Type D	373-049-004	M24308/2-9
Jack	M39024/10-01	M39024/10-01

TABLE VI. PRIMARY AC POWER

Item		Description
Signal Characteristics		
1.	Voltage	120 VAC +/- 10%, single phase
2.	Frequency	57 Hz to 63 Hz; 60 Hz nominal
3.	Power	700 Watts, Maximum
Unit Interface Requirements		
1.	AC power connector shall have only three pins, designated A, B, and C. Within the unit, color coded conductors shall be connected between pins and the first teminals as follows.	

Pin	Conductor Function	Conductor Color*
A	VAC Return	White
B	Saftey Ground	Green
C	VAC Line	Black

* AC power cables may be commercial power cords and connectors which meet equivalent standards for safety and function.

TABLE VII. MIL-STD-1553B DATA BUS

Item		Description
Signal Characteristics		
Signal characteristics as as per MIL-STD-1553B.		
Unit Interface Requirements		
1.	Coupling	Transformer coupled
2.	Remote Terminal Address	The unit Remote Terminal Address for the A Side Bus shall be accomodated via the Primary Interface connector J109. The unit Remote Terminal Address for the B Side Bus shall be accommodated via the Primary Interface connector J111. The Test Modem shall provide internal pull ups for the input signals.
3.	Parity	Odd

TABLE VIII. SETUP AND EXECUTION TIMES

Command	Sync/ Acync	Setup Time	Exec. Time
PTE_SET_STATE_COMMAND	A	N/A	1
PTE_GENERAL_CONFIGURATION_COMMAND	A	N/A	2
PTE_DOWNLOAD_COMMAND	Note 1.		
PTE_EPHEMERIS_DATA_COMMAND	Note 2.		
PTE_DEMOD_SPECIFIC_CONFIGURATION_ COMMAND	A	N/A	2
PTE_DEMOD_COMMON_CONFIGURATION_ COMMAND	A	N/A	2
PTE_DEMOD_START_ACQUISITION_ COMMAND	A	N/A	1
PTE_DEMOD_START_PN_MODEL_COMMAND	S	1	0
PTE_DEMOD_START_FWD_BER_TEST_ COMMAND	A	N/A	1
PTE_DEMOD_RANGE_CHANNEL_ REACQUISITION_COMMAND	A	N/A	1
PTE_MOD_CONFIGURATION_COMMAND	A	N/A	2
PTE_MOD_START_SERVICE_COMMAND	S	1	0
PTE_MOD_START_RTN_BER_TEST_COMMAND	A	N/A	1
PTE_MOD_MEASURE_TIME_INTERVAL_ COMMAND	A	N/A	1

NOTES

1. Not applicable.

2. Ephemeris downloading is subject to 10-10-10 Rule.

3. All times given are in seconds. "Exec. Time" is execution time.

TABLE IX. TEST MODEM COMMAND STATE TABLE

PTE Demod Command State Table Non-Coherent Turnaround	See Table H5-2a.
PTE Modulator Command State Table Non-Coherent Turnaround	See Table H5-2c.
PTE Modem Command State Table Coherent Turnaround	See Table H5-2d.

NOTES

Tables H5-2a., -2c., and -2d. are, by reference, part of Appendix II. They are contained in STGT-HE-06-2, December 1990.

TABLE X. COMMON TIME AND FREQUENCY SYSTEM (CTFS)
10 MHz INPUT

Item		Description
Signal Characteristics		
1.	Nominal frequency	10 MHz
2.	Signal type	Single ended, sinusoidal
3.	Nominal source impedance	50 ohms
4.	Signal level	+ 11 dBm +/- 2 dB into 50 ohms
5.	Single-sideband (SSB) phase noise in 1 Hz bandwidth	
	Frequency Offset From Carrier (Hz)	Phase Noise (dB/Hz)
	0.1	-80
	1	-105
	10	-120
	100	-125
	1,000	-140
6.	Frequency accuracy ($\Delta f/f$)	+/- 4 x 10^{-12}
7.	Frequency stability (square root of zero-dead-time two-sample Allan variance)	
	Averaging Time (Second.)	Stability
	1	< +/- 5.0 x 10-12
	10	< +/- 2.7 x 10-12
	100	< +/- 8.5 x 10-13
8.	Harmonic distortion	less than -50 dBc
9.	Non-harmonically related spurious	less than -80 dBc
Unit Interface Requirements		
1.	Nominal input impedance	50 ohms
2.	Input VSWR	1.3:1 over (10 +/- 0.5) MHz, maximum

TABLE XI. COMMON TIME AND FREQUENCY SYSTEM (CTFS)
1 PULSE PER SECOND (1 PPS) INPUT

Item		Description
Signal Characteristics		
1.	Nominal frequency	1 Hz
2.	Signal type	Single ended, rectangular pulse
3.	Nominal source impedance	50 ohms
4.	Signal levels	TTL levels
5.	Pulse width	100 microseconds, +/- 0.1 %
6.	Rise and fall times	10 nanoseconds, maximum
7.	Pulse to pulse jitter	2 nanoseconds, maximum
8.	Accuracy	< +/- 25 nanoseconds, referenced to the CTFS master epoch
9.	Sense of signal	Time epoch corresponds to the leading edge of the pulse
Unit Interface Requirements		
1.	Nominal input impedance	50 ohms
2.	VSWR	1.3:1, maximum measured from 1 to 35 MHz

TABLE XII. COMMON TIME AND FREQUENCY SYSTEM (CTFS)
TIME OF YEAR (TOY) INPUT

Item		Description
Signal Characteristics		
1.	Nominal frequency	Per IRIG-B Standard, IRIG-STD 104-70
2.	Signal format	IRIG-B level shift
3.	Nominal source impedance	50 ohms
4.	Signal levels	TTL into 50 ohms
5.	Signal type	Single-ended
Unit Interface Requirements		
1.	Nominal input impedance	50 ohms

TABLE XIII. PTE 370 MHz IF OUTPUT

Item	Description
Signal Characteristics	
1. Nominal center frequency	370 MHz
2. Power level	0 dBm +/- 3 dB in a 30 MHz bandwidth
3. Stability of output power	+/- 1 dB over any 1 hour period
4. Spurious signals	
a. Total RSS of all spurious signals	-30 dBc, maximum
b. Individual spurious signals (in or out of band)	-40 dBc, maximum
Unit Interface Requirements	
1. Nominal output impedence	50 ohms
2. Output VSWR	1.3:1, maximum measured over a 19 MHz bandwidth centered at 370 MHz

TABLE XIV. PTE 8.5 MHz IF OUTPUT

Item		Description
Signal Characteristics		
1.	Nominal center frequency	8.5 MHz
2.	Power level	0 dBm +/- 3 dB in a 15 MHz low pass bandwidth
3.	Stability of output power	+/- 1 dB over any 1 hour period
4.	Spurious signals	
a.	Total RSS of all spurious signals	-30 dBc, maximum
b.	Individual spurious signals (in or out of band)	-40 dBc, maximum
Unit Interface Requirements		
1.	Nominal output impedence	50 ohms
2.	Output VSWR	1.3:1, maximum measured between 1 MHz and 10 MHz

TABLE XV. PTE BASEBAND DATA/CLOCK INPUTS

Item		Description
Signal Characteristics		
1.	Data format	NRZ
2.	Data rate	SSA 100 bps to 6 Mbps on I and Q channels; 100 bps to 12 Mbps on I channel for single channel user KSA 1 kbps to 6 Mbps on I and Q channels; 1 kbps to 12 Mbps on I channel for single channel user MA 100 bps to 50 kbps on I and Q channels; 100 bps to 50 kbps on I channel for single channel user
3.	Clock rate	Same as data rate and synchronous with data; Note 1
4.	Source impedence	less than 10 ohms
5.	Signal level	RS-422A; Note 2
6.	Data type	Complimentary balanced differential TTL; Note 2
Unit Interface Requirements		
1.	Input impedance	100 ohms +/- 2% line-to-line for each differential pair

NOTES

1. Data and clock are synchronous unless data is lost in a channel and the data is locked to a logical one.

2. I and Q channels may be independent (asynchronous) with respect to each other.

3. See Figure 18 for Data and Clock relationships.

TABLE XVI. PTE BASEBAND COMMAND DATA/CLOCK OUTPUTS

Item		Description	
Signal Characteristics			
1.	Data format	NRZ	
2.	Data rate	SSA KSA MA	100 bps - 300 kbps 1 kbps - 25 Mbps 100 bps - 10 kbps
3.	Clock rate	Same as data rate and synchronous with data	
4.	Signal type	Similar to RS-422A; see Note 1	
5.	Data type	Complementary balanced differential TTL	
6.	Clock asymmetry	50 +/- 5%, maximum	
7.	Differential voltage level (clock or data)	(A) to (B), 2 volts, minimum	
8.	Time skew (click or data)	(A) to (B), 6.5 ns., maximum	
9.	Time skew (data to clock)	(A) to (A) and (B) to (B) 25% of a bit period, maximum	
10.	20 to 80% differential transition (rise and fall) time (data and clock)	12 ns., maximum	
Unit Interface Requirements			
1.	Output impedance	Less than 10 ohms	

NOTES

1. Clock and data relationships are illustration in figure 18, for definition see table XXXI

TABLE XVII. LOW DATA RATE BASEBAND DATA OUTPUTS

Item	Description
Signal Characteristics	
1. Data format	NRZ or biphase
2. Data rate	1 kpbs to 6 Mbps for NRZ 1 kbps to 3 Mbps for biphase
3. Clock rate (Note 1)	Same as data rate and synchronous with data for NRZ; twice the data rate and synchronous with data for biphase
4. Signal level	RS-422A
5. Signal type	Complementary balanced differential TTL
6. Clock asymmetry	50 +/- 5%, maximum
7. Differential voltage level (clock or data)	(A) to (B), 2 volts, minimum
8. Time skew (clock or data)	(A) to (B), 6.5 ns., maximum
9. Time skew (data to clock)	(A) to (A) and (B) to (B) 25 % of a bit period, maximum
10. 20 to 80 % differential transition (rise and fall) time (data and clock)	12 ns., maximum
Unit Interface Requirements	
1. Output impedance	Less than 10 ohms

NOTES

1. Clock and data relationships are illustrated in figure 18, for definition see table XXXI

TABLE XVIII. I AND Q SIMULATED USER RETURN
DATA AND CLOCK INPUTS

Item	Description
Signal Characteristics	
1. Data format	NRZ
2. Data rate	100 bps to 6 Mbps on I and Q channels; 100 bps to 12 Mbps on I channel for single channel user
3. Clock rate	Same as data rate and synchronous with data
4. Signal level (clock or data) (Note 1)	Differential (A) to (B) voltage, 400 mV, minimum
5. Signal type (Note 1)	Complementary balanced differential TTL
6. Nominal source impedance	Less than 10 ohms
7. Clock asymmetry	50 +/- 5 % maximum
8. Time skew (data to clock)	(A) to (A) and (B) to (B), 25 % of a bit period, maximum
9. Time skew (data or clock)	(A) to (B) 6.5 ns., maximum
10. Transition time, 20 to 80 % differential (data and clock)	18 ns, maximum
Unit Interface Requirements	
1. Output impedance differential signal pair	100 ohms +/- 2% line-to-line for each

NOTES

1. Signals are similar to RS-422A but extend beyond 10 MHz.

2. The receiver driver chip set used is an SN75ALS191 Texas Instruments line driver and a DS26C32ACJ National Semiconductor line receiver. Equivalent or better circuits may be used.

3. Clock and data relationships are illustrated in Figure 18, for definition see table XXXI

TABLE XIX. RECOVERED FORWARD DATA AND CLOCK OUTPUTS

Item	Description
Signal Characteristics	
1. Data format	NRZ
2. Data rate	100 bps to 25 Mbps
3. Clock rate	Same as data rate and synchronous with data
4. Signal level (clock or data)	Differential (A) to (B) voltage, 400 mV, minimum
5. Signal type	Complementary balanced differential TTL
6. Nominal source impedance	Less than 10 ohms
7. Clock asymmetry	50 +/- 5 % maximum
8. Time skew (data to clock)	(A) to (A) and (B) to (B), 6.5 ns, maximum
9. Transition time, 20 to 80 % differential (data and clock)	18 ns, maximum
Unit Interface Requirements	
1. Output impedance	Less than 10 ohms

NOTES

1. Signals are similar to RS-422A but extend beyond 10 MHz.

2. The receiver driver chip set used is an SN75ALS191 Texas Instruments line driver and a DS26C32ACJ National Semiconductor line receiver. Equivalent or better circuits may be used.

3. Clock and data relationship are illustrated in Figure 18, for definition see table XXXI

TABLE XX. PTE 370 MHz IF INPUT

Item	Description
Signal Characteristics	
1. Nominal center frequency	370 MHz
2. Nominal source impedance	50 ohms
3. Spurious signals	
a. Total RSS of all spurious signals	-30 dBc, maximum
b. Individual spurious signals in and out of band	-40 dBc, maximum
Unit Interface Requirements	
1. Nominal input impedance	50 ohms
2. VSWR	1.3:1, maximum measured over a 30 MHz band centered about 370 MHz
3. Connector type and location	See table II.

TABLE XXI. TRANSMIT CLOCK OUTPUTS

Item	Description
Signal Charcteristics	
1. Clock rate	100 Hz to 25 MHz for Command Channel BERTS; 100 Hz to 12 MHz for I and Q channel BERTS
2. Signal level	TTL
3. Signal type	Unbalanced single-ended TTL

TABLE XXII. DATA INPUTS

Item		Description
Signal Charcteristics		
1.	Data rate	100 bps to 25 bps for Command Channel BERTS; 100 bps to 12 Mbps for I and Q channel BERTS
2.	Signal level	TTL
3.	Signal type	Unbalanced single-ended TTL
4.	Data format	NRZ

TABLE XXIII. RECOVERED DATA AND CLOCK OUTPUTS

Item	Description
Signal Charcteristics	
1. Data and clock rate	100 bps to 25 bps for Command Channel BERTS; 100 bps to 12 Mbps for I and Q channel BERTS. Clock rate is identical to and synchronous with the data rate
2. Signal level	TTL
3. Signal type	Unbalanced single-ended TTL
4. Data format	NRZ

TABLE XXIV. TEST MODEM 70 MHz (SIGNAL) OUTPUT

Item	Description
Signal Characteristics	
1. Nominal center frequency	70 MHz
2. Power level (Note 1)	-55 dBm to +10 dBm
Unit Interface Requirements	
1. Connector type and location	See table II.

NOTES

1. Power level is signal only and is referenced to the Test Modem's output port.

TABLE XXV. TEST MODEM 70 MHz (SIGNAL + NOISE) INPUT

Item	Description
Signal Characteristics	
1. Nominal center frequency	70 MHz
2. Power level (Note 1)	-55 dBm to +10 dBm
Unit Interface Requirements	
1. Connector type and location	See table II.

NOTES

1. The power at the Test Modem input is either signal or signal plus AWGN at the Test Modem's input port.

TABLE XXVI. ALLOWABLE IMPLEMENTATION LOSS

Allowable Implementation Loss, $L(P_E, Rb)$, at Various Theoretical Eb/No Reference Points for USS Forward Services (Losses are in units of dB)			
Reference Points for Uncoded Data Rate 1/3 Coded	$P_E = 10^{-5}$ @ 9.6 dB @ 3.9 dB	$P_E = 10^{-6}$ @ 10.6 dB @ 4.5 dB	$P_E = 10^{-7}$ @ 11.5 dB @ 5.1 dB
	SSA Forward, Uncoded		
100 bps $\leq$ Rb < 1 kbps	4.0	4.5	5.0
1 kbps $\leq$ Rb $\leq$ 300 kbps	3.5	4.0	4.5
	KSA Forward, Uncoded (Including K-Shuttle)		
1 kbps $\leq$ Rb < 1 Mbps	3.5	4.0	4.5
1 Mbps $\leq$ Rb < 6 Mbps	4.0	4.5	5.0
6 Mbps $\leq$ Rb $\leq$ 25 Mbps	6.0	6.5	7.0
	MA Forward, Uncoded		
100 bps $\leq$ Rb $\leq$ 10 kbps	3.5	4.0	4.5
	S-Shuttle Forward, Rate 1/3 Convolutional Coding		
32 kpbs or 72 kbps	4.0	4.5	5.0

TABLE XXVII. INPUT PHASE NOISE

	Maximum Phase Noise in Degrees, RMS		
	SSAF	KSAF	MAF
Internal Test Loops			
1 Hz - 10 Hz	2.0	2.0	2.0
10 Hz - 32 Hz	2.0	2.0	2.0
32 Hz - 1 kHz	5.6	5.6	5.6
1 kHz - 3 MHz	NA	NA	1.5
1 kHz - 10 MHz	1.5	NA	NA
1 kHz - 25 MHz	NA	1.5	NA
End-to-End Test Loops			
1 Hz - 10 Hz	2.5	15.1	2.5
10 Hz - 1 kHz	5.9	11.0	5.9
1 kHz - 3 MHz	NA	NA	2.3
1 kHz - 10 MHz	2.3	NA	NA
1 kHz - 25 MHz	NA	2.9	NA

TABLE XXVIII. INPUT FREQUENCY DYNAMICS

	Frequency[1] Range (kHz)	Frequency Rate (Hz/s)	Frequency Acceleration (Hz/s^2)
SSAF and SSHF	- 835 to + 335	+/- 360	+/- 15
KSAF and KSHF	- 1,260 to + 1,260	+/- 700	+/- 1.0
MAF	- 185 to + 1,585	+/- 112	+/- 0.15

NOTES

1. Frequency range is with respect to a 370.0 MHz center frequency.

TABLE XXIX. ACQUISITION TIMES AND C/No

	Service Mode	Input C/No (dB-Hz)	Aquisition Time (s)
1.	Internal Loopback Tests		
a.	SSAF	100	1.0
b.	SSHF	100	1.0
c.	KSAF	100	1.0
d.	KSHF	100	1.0
e.	MAF	100	1.0
2.	End-to-End Loopback Tests		
a.	SSAF	40 or C/No_{MIN}, whichever is greater	10.0
b.	SSHF	C/No_{MIN}	20.0
c.	KSAF, data rates up to 6 Mbps	40 or C/No_{MIN}, whichever is greater	10.0
d.	KSAF, data rates > 6 Mbps	C/No_{MIN}	25.0
e.	KSHF	C/No_{MIN}	5.0
f.	MAF	40 or C/No_{MIN}, whichever is greater	10.0

NOTES

1. C/No_{MIN} is the minimum total C/No at the IF input to the Test Modem Forward Demodulator for which a P_E of 10^{-5} is specified for the given configuration.

TABLE XXX. PROFILE LIMITS ON $df_{RM}(t)$

	Frequency[1] Range (kHz)	Frequency Rate (Hz/s)	Frequency Acceleration (Hz/s^2)
SSAR and SSHR	- 600 to + 490	+/- 770	+/- 31
KSAR and KSHR	- 1,972 to + 1,972	+/- 1,500	+/- 2.0
MAR	- 240 to + 190	+/- 240	+/- 13

NOTES

1. For KSAR and KSHR, the sum of $df_{RM}(t)$ and dfm will lie in the specified frequency range.

TABLE XXXI. TIMING PARAMETERS

PARAMETER	REQUIREMENT
Clock Asymmetry	50 ±5 percent, MAX.
Differential (A) to (B) voltage (clock or data)	2.0 V, MIN
Time Skew (A) to (B) (data or clock)	6.5 ns, MAX
Time Skew (A) to (A) and (B) to (B) (data to clock)	25 percent of a bit period, MAX
20 to 80 percent differential transition time (data and clock)	12 ns, MAX

DEFINITIONS

A. SPECIFIED PARAMETERS

See figure F-18 for an illustration of the parameters defined as follows:

1. CLOCK ASYMMETRY. This parameter specifies the allowable clock duty cycle range around 50 percent.

2. DIFF (A) TO (B) VOLT. This parameter specifies the allowable plus or minus differential voltage to ensure a voltage at the receiver input capable of producing a full receiver output swing.

3. TIME SKEW (A) TO (B). This parameter identifies the alowed time skew between the (A) cable and the (B) cable of any differentially transmitted signal. The total time skew varies linearly along the total cable length. The total time skew is the difference between the driver output skew and worst case receiver input skew.

4. TIME SKEW (A) DATA TO (A) CLOCK. This parameter identifies the allowed time skew between a clock signal (A Cable) and its related data signal or signals (A Cable). This parameter is evaluated on an instantaneous clock period to data period basis. It includes all combination effects of clock asymmetry and jitter conditions in their total affect on clock transition and data midpoint skew.

B. LOGICAL SENSE

The logical signal exchange between the driver and receiver shall be in accordance with the following convention for balanced differential interfaces:

1. The (A) terminal of the driver shall be negative with respect to the (B) terminal for binary 1 exchange.

2. The (A) terminal of the driver shall be positive with respect to the (B) terminal for a binary 0 exchange.

3. The significant transition for the clock signal is the negative-going transition of the A-line with respect to the B-line. This transition shall occur within the specified tolerance of the midpoint of data bit period.

4. All data crossings shall be coincident with the positive going clock transitions.

Appendix I

10.0 SIGNAL PARAMETERS AND CONSTRAINTS

10.1 SCOPE

This appendix provides detailed descriptions of signal parameters and constraints for STGT User Service Subsystem (USS) forward and return data supported by the Test Modem in the S-band Single Access (SSA), K-band Single Access (KSA) and Multiple Access (MA) receiver equipment.

10.2 RETURN SIGNAL PARAMETERS AND CONSTRAINTS

This section provides the data format and channel encoding for SSA, KSA and MA return links, including S-band and K-band shuttle.

10.2.1 Return Signal Formats

10.2.1.1 SSA and SSHR Signal Formats

10.2.1.1.1 SSA DG-1 Mode 1

1. Single data channel data rate restrictions

Uncoded, NRZ	0.1 to 300 kbps	
Uncoded, Biphase	0.1 to 300 kbps	
Coded (r = 1/2), NRZ	0.1 to 150 kbps	PN/BPSK, SQPN/QPSK
Coded (r=1/2), Biphase	0.1 to 75 kbps	PN/BPSK, SQPN/QPSK
Coded (r = 1/2), NRZ	1 to 300 kbps	SQPN/SQPSK
	Alternate Data Bits	

2. Dual data channel (QPSK) I and Q channel data rate restrictions:

Uncoded, NRZ	0.1 to 300 kbps
Uncoded, Biphase	0.1 to 150 kbps
Coded (r = 1/2), NRZ	0.1 to 150 kbps
Coded (r = 1/2), Biphase	0.1 to 75 kbps

   a. Data signals on the I and Q channels may be independent and asynchronous.

3. Data Format — NRZ-L,M,S; Biphase - L,M,S

   a. Data format is independent for the I and Q channels.
   b. Biphase for uncoded operation only.

4. Symbol Format — NRZ-L, Biphase-L

   a. When NRZ channel symbols are used, the G2 symbols may be normal or inverted, as commanded.

   b. G2 symbols are always normal polarity for biphase.

   c. Symbol format is independent for the I and Q channels.

5. Encoding and Interleaving Code 1

a. Symbols generated from G1 will precede symbols generated from G2 relative to the data bit period.

b. No symbol interleaving is required for this mode.

6. Data Modulation

PN/BPSK	Single data channel
SQPN/SQPSK or SQPN/UQPSK	Single or dual data channel
SQPSK	Single data channel alternate symbols

7. I/Q Power Imbalance

1:1, 1:2, or 1:4

8. PN Coding

Length	(2^10 - 1) x 256 chips
Code Family	Truncated 18-stage shift register per STDN 108
Chip Rate	As per 3.2.1.2.6
Epoch Reference	
I channel	Synchronous with Forward Range Channel (coupled mode) or commanded 1-pps
Q channel	Delayed (x+1/2) chips relative to I-Channel Epoch, where x is determined by the user spacecraft ID per STDN 103

10.2.1.1.2 <u>SSA DG-1 Mode 2</u>

1. Single data channel data rate restrictions

Uncoded, NRZ	1 to 300 kbps
Uncoded, Biphase	1 to 300 kbps
Coded (r = 1/2), NRZ	1 to 150 kbps PN/BPSK, SQPN/QPSK
Code (r = 1/2), Biphase	1 to 75 kbps PN/BPSK, SQPN/QPSK
Coded (r = 1/2), NRZ	1 to 300 kbps SQPN/SQPSK Alternate data bits

2. Dual data channel (QPSK) I and Q channel data rate restrictions:

Uncoded, NRZ	1 to 300 kbps
Uncoded, Biphase	1 to 150 kbps
Coded (r = 1/2), NRZ	1 to 150 kbps
Code (r = 1/2), Biphase	1 to 75 kbps

a. Data signals on the I and Q channels may be independent and asynchronous.

3. Data Format NRZ-L,M,S: Biphase-L,M,S

a. Data format is independent for the I and Q channels.
b. Biphase for uncoded operation only.

4. Symbol Format NRZ-L, Biphase-L

a. When NRZ channel symbols are used, the G2 symbols may be normal or inverted, as commanded.

b. G2 symbols are always normal polarity for biphase.

c. Symbol format is independent for the I and Q channels.

5. Encoding and Interleaving Code 1

a. Symbols generated from G1 will precede symbols generated from G2 relative to the data bit period.

b. No symbol interleaving is required for this mode.

6. Data Modulation

PN/BPSK	Single data channel
SQPN/SQPSK or SOPN/UQPSK	Single or dual data channel
SQPSK	Single data channel alternate symbols

7. I/Q Power Imbalance

1:1, 1:2, or 1:4

8. PN Coding

Length	2^11 - 1 chips
Code Family	Gold codes per STDN 108
Chip Rate	As per 3.2.1.2.6
Epoch Reference	
I channel	Synchronous with the Forward Range Channel (coupled mode) or commanded 1-pps mark (uncoupled).
Q channel	Delayed 1/2 chip relative to I-Channel Epoch.

10.2.1.1.3 <u>SSA DG-1 Mode 3</u>

1. Dual data channel (QPSK) I and Q channel data rate restrictions:

I Channel (PN Spread)

Uncoded, NRZ	0.1 to 300 kbps
Uncoded, Biphase	0.1 to 150 kbps
Coded (r = 1/2), NRZ	0.1 to 150 kbps
Coded (r = 1/2), Biphase	0.1 to 75 kbps

Q Channel

Uncoded, NRZ	1 kbps to 6 Mbps
Uncoded, Biphase	1 kbps to 3 Mbps
Coded (r = 1/2), NRZ	1 kbps to 3 Mbps
Coded (r = 1/2), Biphase	1 kbps to 1.5 Mbps
Coded (r = 1/3), NRZ	1 kbps to 2 Mbps
Coded (r = 1/3), Biphase	1 kbps to 1 Mbps

a. Data signals on the I and Q channels are independent and asynchronous.

3. Data Format — NRZ-L,M,S: Biphase-L,M,S

a. Data format is independent for the I and Q channels.
b. Biphase for uncoded operation only.

4. Symbol Format — NRZ-L, Biphase-L

a. When NRZ channel symbols are used, the G2 symbols may be normal or inverted, as commanded.

b. G2 symbols are always normal polarity for biphase.

c. Symbol format is independent for the I and Q channels.

5. Encoding and Interleaving

a. Code 1; independent for the I and Q channel. Code 3 for Q channel only.

b. Interleaving may be used for symbol rates exceeding 300 ksps for the Q channel.

6. Data Modulation: PN/QPSK or PN/UQPSK

7. I/Q Power Imbalance

1:1, 1:2, or 1:4

8. PN Coding

Length	(2^10 - 1) x 256 chips
Code Family	Truncated 18-stage shift register per STDN 108 (I channel only)
Chip Rate	As per paragraph 3.?.1.2.6.

Epoch Reference

I channel	Synchronous with Forward Range Channel (coupled mode) or commanded 1-pps mark (uncoupled)

10.2.1.1.4 SSA DG-2

1. Single data channel data rate restrictions (SQPSK)

   a. Alternate I/Q encoded symbols

Code (r = 1/2), NRZ	1 to 300 kbps

   b. Alternate I/Q data bits

Uncoded, NRZ	1 to 12000 kbps
Coded (r = 1/2), NRZ	1 to 6000 kbps
Coded (r = 1/3), NRZ	1 to 4000 kbps

   c. Interleaving may be commanded only for symbol rates above 300 ksps, coded, NRZ.

   d. I symbols precede Q symbols by one-half symbol.

   e. G2 symbols from the encoder may be normal or inverted, as commanded.

2. Single data channel data rate restrictions 9BPSK)

Uncoded, NRZ	1 to 6000 kbps
Uncoded, biphase	1 to 3000 kbps
Coded (r = 1/2), NRZ	1 to 3000 kbps
Coded (r = 1/2), Biphase	1 to 1500 kbps
Coded (r = 1/2), NRZ	1 to 2000 kbps
Coded (r = 1/3), biphase	1 to 1000 kbps

   a. Interleaving may be commanded only for symbol rates above 300 ksps, coded, NRZ.

   b. For NRZ symbols, G2 symbols from the encoder may be normal or inverted, as commanded.

   c. For biphase symbols, G2 symbols are always normal polarity.

   d. G1 symbols are always inverted for code 2.

3. Dual data channel (QPSK) I and Q channel data rate restrictions:

Uncoded, NRZ	1 to 6000 kbps
Uncoded, biphase	1 to 3000 kbps
Coded (r = 1/2), NRZ	1 to 3000 kbps
Coded (r = 1/2), Biphase	1 to 1500 kbps
Coded (r = 1/3), NRZ	1 to 2000 kbps

a. Data signals on the I and Q channels may be independent and asynchronous.

b. Interleaving may be commanded only for symbol rates above 300 ksps, coded, NRZ.

c. For NRZ, G2 symbols may be normal or inverted, as commanded.

d. For biphase, G2 symbols are always normal polarity.

4. Data Format NRZ-L,M,S: Biphase-L,M,S

a. Data format is independent for the I and Q channels.
b. Biphase formats for uncoded operation only.

5. Symbol Format NRZ-L, Biphase-L

a. Symbol format is independent for the I and Q channels.

6. Encoding and Interleaving

a. Code 1: Single data channels (SQPSK or BPSK) and dual data channels.

b. Code 2: Single data channel (BPSK only).

c. Code 3: Single data channels (SQPSK or BPSK) and dual data channels.

7. Data Modulation

BPSK	Single data channel
SQPSK	Single data channel
QPSK/UQPSK	Dual data channel

8. I/Q Power Imbalance

a. 1:1 QPSK and SQPSK
b. 4:1 UQPSK

10.2.1.1.5 SSHR

1. Data rate restrictions

a. Mode 1

Coded (r = 1/3), Biphase 96 kbps

b. Mode 2

Coded (r = 1/3), Biphase 192 kbps

c. Mode 3: No data, CW only.

2. Data Format NRZ-L

3. Symbol Format Biphase-L

4. Encoding — Code 4

a. Interleaving is never used in this mode.

5. Data Modulation — BPSK

10.2.1.2 KSA and KSHR Return Signals

10.2.1.2.1 KSA DG-1 Mode 1

1. Single data channel data rate restrictions

Uncoded, NRZ	1 to 300 kbps
Uncoded, Biphase	1 to 150 kbps
Coded (r = 1/2), NRZ	1 to 150 kbps
Coded (r = 1/2), Biphase	1 to 75 kbps

2. Dual data channel (QPSK) I and Q channel data rate restrictions:

Uncoded, NRZ	1 to 300 kbps
Uncoded, Biphase	1 to 150 kbps
Coded (r = 1/2), NRZ	1 to 150 kbps
Coded (r = 1/2), Biphase	1 to 75 kbps

a. Data signals on the I and Q channels may be independent and asynchronous.

3. Data Format — NRZ-L,M,S; Biphase-L,M,S

a. Data format is independent for the I and Q channels.
b. Biphase for uncoded operation only.

4. Symbol Format — NRZ-L, Biphase-L

a. When NRZ channel symbols are used, the G2 symbols may be normal or inverted, as commanded.

b. G2 symbols are always normal polarity for biphase.

c. Symbol format is independent for the I and Q channels.

5. Encoding and Interleaving — Code 1

a. Symbols generated from G1 will precede symbols generated from G2 relative to the data bit period.

b. No symbol interleaving is required for this mode.

6. Data Modulation

PN/BPSK	Single data channel
SQPN/QPSK or SQPN/UQPSK	Single or dual data channel

7. I/Q Power Imbalance

1:1, 1:2, or 1:4

8. PN Coding

Length	(2^10 - 1) x 256 chips
Code Family	Truncated 18-stage shift register per STDN 108
Chip Rate	As per 3.2.1.2.6
Epoch Reference	
I channel	Synchronous with Forward Range Channel (coupled mode) or commanded 1-pps mark (uncoupled)
Q channel	Delayed (x+1/2) chips relative to I-Channel Epoch. Where X is determined by the user spacecraft ID per STDN 108.

10.2.1.2.2 KSA DG-1 Mode 2

1. Single data channel data rate restrictions

Uncoded, NRZ	1 to 300 kbps
Uncoded, Biphase	1 to 150 kbps
Coded (r = 1/2), NRZ	1 to 150 kbps
Coded (r = 1/2), Biphase	1 to 75 kbps

2. Dual data channel (QPSK) I and Q channel data rate restrictions:

Uncoded, NRZ	1 to 300 kbps
Uncoded, Biphase	1 to 150 kbps
Coded (r = 1/2), NRZ	1 to 150 kbps
Coded (r = 1/2), Biphase	1 to 75 kbps

a. Data signals on the I and Q channels may be independent and asynchronous.

3. Data Format NRZ-L,M,S; Biphase-L,M,S

a. Data format is independent for the I and Q channels.
b. Biphase for uncoded operation only.

4. Symbol Format NRZ-L, Biphase-L

a. When NRZ channel symbols are used, the G2 symbols may be normal or inverted, as commanded.

b. G2 symbols are always normal polarity for biphase.

c. Symbol format is independent for the I and Q channels.

5. Encoding and Interleaving — Code 1

a. Symbols generated from G1 will precede symbols generated from G2 relative to the data bit period.

b. No symbol interleaving is required for this mode.

6. Data Modulation

PN/BPSK	Single data channel
SQPN/QPSK or SQPN/UQPSK	Single or dual data channel

7. I/Q Power Imbalance

1:1, 1:2, or 1:4

8. PN Coding

Length	2^11 - 1 chips
Code Family	Gold codes per STDN 108
Chip Rate	As per 3.2.1.2.6
Epoch Reference	
I channel	Synchronous with Forward Range Channel (coupled mode) or commanded 1-pps mark (uncoupled)
Q channel	Delayed 1/2 chip relative to I-Channel Epoch

10.2.1.2.3 <u>KSA DG-1 Mode 3</u>

1. Dual data channel (QPSK) I and Q channel data rate restrictions:

I Channel (PN Spread)

Uncoded, NRZ	0.1 to 300 kbps
Uncoded, Biphase	0.1 to 150 kbps
Coded (r = 1/2), NRZ	0.1 to 150 kbps
Coded (r = 1/2), Biphase	0.1 to 75 kbps

Q Channel

Uncoded, NRZ	1 kbps to 6 Mbps
Uncoded, Biphase	1 kbps to 3 Mbps
Coded (r = 1/2), NRZ	1 kbps to 3 Mbps
Coded (r = 1/2), Biphase	1 kbps to 1.5 Mbps

a. Data signals on the I and Q channels are independent and asynchronous.

3. Data Format — NRZ-L,M,S: Biphase-L,M,S

a. Data format is independent for the I and Q channels.
b. Biphase for uncoded operation only.

4. Symbol Format — NRZ-L, Biphase-L

a. When NRZ channel symbols are used, the G2 symbols may be normal or inverted, as commanded.

b. G2 symbols are always normal polarity for biphase.

c. Symbol format is independent for the I and Q channels.

5. Encoding and Interleaving

a. Code 1

6. Data Modulation: QPSK dual data channel

7. I/Q Power Imbalance

1:1, 1:2, or 1:4

8. PN Coding

Length	(2^10 - 1) x 256 chips
Code Family	Truncated 18-stage shift register per STDN 108 (I channel only)
Chip Rate	As per 3.2.1.2.6
Epoch Reference	
I channel	Synchronous with Forward Range Channel (coupled mode) or commanded 1-pps mark (uncoupled)

10.2.1.2.4 KSA DG-2

1. Single data channel data rate restrictions (Uncoded, SQPSK)

Uncoded, NRZ — 1 to 12000 kbps

a. I and Q channels consist of alternate bits of a single data channel.

b. I and Q channels will be separately differentially formatted prior to modulation.

c. I symbols precede Q symbols by one-half symbol.

2. Single data channel data rate restrictions (Coded SQPSK)

Coded (r = 1/2), NRZ	1 to 6000 kbps

a. I symbols precede Q symbols by one-half symbol.

b. Single data channel contains two concurrent output symbols of the convolutional encoder on the I and Q channels.

3. Single data channel data rate restrictions (BPSK)

Uncoded, NRZ	1 to 6000 kbps
Uncoded, biphase	1 to 3000 kbps
Coded (r = 1/2), NRZ	1 to 3000 kbps
Coded (r = 1/2), Biphase	1 to 1500 kbps

4. Dual data channel (QPSK) I and Q channel data rate restrictions:

Uncoded, NRZ	1 to 6000 kbps
Uncoded, biphase	1 to 3000 kbps
Coded (r = 1/2), NRZ	1 to 3000 kbps
Coded (r = 1/2), Biphase	1 to 1500 kbps

a. Data signals on the I and Q channels may be independent and asynchronous.

b. Either data signal may be uncoded or convolutionally encoded.

5. Data Format NRZ-L,M,S: Biphase-L,M,S

a. Data format is independent for the I and Q channels.
b. Biphase for uncoded operation only.

6. Symbol Format NRZ-L, Biphase-L

a. Symbol format is independent for the I and Q channels.

7. Encoding and Interleaving

a. Code 1: Single data channels (SQPSK OR BPSK) and dual data channels.

8. Data Modulation

BPSK	Single data channel
SQPSK	Single data channel
QPSK/UQPSK	Dual data channel

9. I/Q Power Imbalance

a. 1:1 QPSK and SQPSK
b. 4:1 UQPSK

10.2.1.2.5 KSHR

1. Mode 1 and mode 2 data rate restrictions

I channel	16 to 2000 kbps
Q channel	192 kpbs

2. Data Format NRZ-L,M,S; Biphase L,M,S

   a. Data format is independent for the I and Q channels
   b. This mode is always uncoded.

3. I/Q Power Ratio is 4:1

10.2.1.3 Multiple Access Return Signals

10.2.1.3.1 MA DG-1 Mode 1

1. Single data channel data rate restrictions

Coded (r = 1/2), NRZ	0.1 to 50 kbps
Coded (r = 1/2), Biphase	0.1 to 50 kbps

2. Dual data channel (QPSK) I and Q channel data rate restrictions:

Coded (r = 1/2), NRZ	0.1 to 50 kbps
Coded (r = 1/2), Biphase	0.1 to 50 kbps

   a. Data signals on the I and Q channels may be independent and asynchronous. If independent, the sum of the I and Q data rates shall not exceed 50 kbps.

3. Data Format NRZ-L,M,S

   a. Data format is independent for the I and Q channels.

4. Symbol Format NRZ-L, Biphase-L

   a. When NRZ channel symbols are used, the G2 symbols may be normal or inverted, as commanded.

   b. G2 symbols are always normal polarity for biphase.

   c. Symbol format is independent for the I and Q channels.

5. Encoding and Interleaving Code 1

   a. Symbols generated from G1 will precede symbols generated from G2 relative to the data bit period.

   b. No symbol interleaving is required for this mode.

6. Data Modulation

PN/BPSK	Single data channel
SQPN/QPSK or SQPN/UQPSK	Single or dual data channel

7. I/Q Power Imbalance

1:1, 1:2, or 1:4

8. PN Coding

Length	(2^10 - 1) x 256 chips
Code Family	Truncated 18-stage shift register per STDN 108
Chip Rate	As per 3.2.1.2.6
Epoch Reference	
I channel	Synchronous with Forward Range Channel (coupled mode) or commanded 1-pps
Q channel	Delayed (x+1/2) chips relative to I-Channel Epoch. Where X is determined by the user spacecraft ID per STDN 108.

10.2.1.3.2 <u>MA DG-1 Mode 2</u>

1. Single data channel data rate restrictions

Coded (r = 1/2), NRZ	1 to 50 kbps
Code (r = 1/2), Biphase	1 to 50 kbps

2. Dual data channel (QPSK) I and Q channel data rate restrictions:

Coded (r = 1/2), NRZ	1 to 50 kbps
Code (r = 1/2), Biphase	1 to 50 kbps

a. Data signals on the I and Q channels may be independent and asynchronous. If independent, the sum of the I and Q data rates shall not exceed 50 kbps.

3. Data Format NRZ-L,M,S

a. Data format is independent for the I and Q channels.

4. Symbol Format NRZ-L, Biphase-L

a. When NRZ channel symbols are used, the G2 symbols may be normal or inverted, as commanded.

b. G2 symbols are always normal polarity for biphase.

c. Symbol format is independent for the I and Q channels.

5. Encoding and Interleaving — Code 1

   a. Symbols generated from G1 will precede symbols generated from G2 relative to the data bit period.

   b. No symbol interleaving is required for this mode.

6. Data Modulation

PN/BPSK	Single data channel
SQPN/QPSK or SQPN/UQPSK	Single or dual data channel

7. I/Q Power Imbalance

   1:1, 1:2, or 1:4

8. PN Coding

Length	2^11 - 1 chips
Code Family	Gold codes per STDN 108
Chip Rate	As per 3.2.1.2.6
Epoch Reference	
I channel	Synchronous with Forward Range Channel (coupled mode) or commanded 1-pps mark (uncoupled)
Q channel	Delayed 1/2 chip relative to I-Channel Epoch

10.3 FORWARD SIGNAL PARAMETERS AND CONSTRAINTS

This section provides the data format and channel encoding for SSA< KSA and MA forward lines, including S-band and K-band shuttle.

10.3.1 Forward Signal Formats

10.3.1.1 SSA Signal Formats

1. Data rate restrictions

   Uncoded, NRZ — 0.1 to 300 kbps

2. Data Format — NRZ-L,M,S) Note: The Forward Demodulator is not required to perform data format conversions for SSAF)

3. Symbol Format — None

4. Encoding — None

5. Data Modulation

UQPSK	Range channel has no data, PN only.
BPSK	If PN disabled.

6. I/Q Power Imbalance

10 db

7. PN coding (PN may be disabled)

Length	Range: (2^10 - 1) x 256 chips Command: (2^10 - 1) chips
Code Family	Range: Truncated 18-stage shift register per STDN 108 Command: Gold Codes per STDN 108
Chip Rate	Coherently related to carrier per MDP requirements
Epoch Reference Range channel	All 1's condition time synchronized to the Command Channel PN code epoch.

10.3.1.2 <u>SSHF Signal Formats</u>

1. Data rate restrictions

a. Mode 1

Coded (r = 1/3), Biphase — 32 kbps

b. Mode 2

Code (r = 1/3), Biphase — 72 kbps

2. Data Format — NRZ-L

3. Symbol Format — Biphase-L

4. Encoding — Code 4

a. Interleaving is never used in this mode.

5. Data Modulation — BPSK

6. PN Coding (PN may be disabled)

Length	1023 chips
Code Family	Per STDN 108
Chip Rate	11:232 M chips per second, nominal

10.3.1.3 KSA Signal Formats

1. Data rate restrictions

Uncoded, NRZ	1 kbps to 25 M bps
2. Data Format	NRZ-L,M,S (Note: The Forward Demodulator is not required to perform data format conversions for KSAF)
3. Symbol Format	None
4. Encoding	None
5. Data Modulation	
UQPSK	Range channel has no data, PN only.
BPSK	For data rates > 300 Kbps, PN off
BPSK	If PN disabled
6. I/Q Power Imbalance	
10 dB	
7. PN Coding	(PN may be disabled)
Length	Range: (2^10 - 1) x 256 chips Command: (2^10 - 1) chips
Code Family	Range: Truncated 18-stage shift register per STDN 108 Command: Gold Codes per STDN 108
Chip Rate	Coherently related to carrier per MDP requirements.
Epoch Reference Range channel	All 1's condition time synchronized to the Command Channel PN code epoch.

Note: Command and Range channel PN modulations will be inhibited for data rates exceeding 300 Kbps.

10.3.1.4 KSHF Signal Formats

1. Data rate restrictions	Mode 1: 216 Kbps Mode 2: 72 Kbps
2. Data Format	Bi-phase-L
3. Symbol Format	None
4. Encoding	None

5.	Data Modulation	BPSK
6.	PN Coding	(PN may be disabled)
	Length	(2^10 - 1) chips
	Code Family	Forward link command channel codes from STDN 108
	Chip Rate	Coherently related to carrier per MDP requirements

10.3.1.5 <u>MA Signal Formats</u>

1.	Data rate restrictions	
	Uncoded, NRZ	0.1 to 10 kbps
2.	Data Format	NRZ-L,M,S (Note: The Forward Demodulator is not required to perform data format conversions for MAF)
3.	Symbol Format	None
4.	Encoding	None
5.	Data Modulation	
	UQPSK BPSK	Range channel has no data, PN only. If PN disabled
6.	I/Q Power Imbalance	
	10 dB	
7.	PN Coding	(PN may be disabled)
	Length	Range: (2^10 - 1) x 256 chips Command: (2^10 - 1) chips
	Code Family	Range: Truncated 18-stage shift register per STDN 108 Command: Gold Codes per STDN 108
	Chip Rate	Coherently related to carrier per MDP requirements
	Epoch Reference Range channel	All 1's condition time synchronized to the Command Channel PN code epoch.

10.3.2 Coding Characteristics

The PTE shall support the following convolutional decoding modes for use with S-Shuttle service type, only:

a. Code 4

1. Convolutional, non-systematic, non-transparent
2. Rate 1/3, constraint length 7
3. Generator functions:

   G1 = 1111001
   G2 = 1011011
   G3 = 1100101

4. Symbol sequence from the convolutional coding will be symbols generated from G1, G2 and G3 successively relative to the data bit period.

5. The encoded symbols will have been format converted to biphase-L.

APPENDIX II

20.0 Not Used

APPENDIX III

30.0 TRACEABILITY MATRIX

30.1 SCOPE

This appendix provides a matrix that traces unit level requirements from this specification, 7472506, to requirements given in General Electric Corporation Hardware Configuration Item (HWCI) Specification, GES-STGT-1323, -1325, and -1328. The unit is required to satisfy, as a minimum, the requirements of these specifications for a Test Modem.

30.2 TRACEABILITY

30.2.1 Direct Traceability

All Test Modem requirements in 7472506 shall be traceable to the reference GE HWCI specifications, either directly, or through a set of logically derived requirements.

30.2.2 Single Configuration Item

The Test Modem constitutes a single configuration item and may be used interchangeably in the K-Band Single Access Low Data Rate Equipment, S-Band Single Access Equipment, or Multiple Access Receiver/Transmit Equipment of the User Services Subsystem (USS) in the Second TDRSS Ground Terminal. As such, each GE HWCI requirement is satisfied by the unit, but not each unit requirement traces back to all of the HWCI specifications, since not all of these configuration items require all of the unit's capabilities.

30.3 THE MATRIX

The traceability matrix is presented in the following table.

REQUIREMENTS TRACEABILITY MATRIX

This matrix provides a trace of requirements from the GE HWCI specifications for SSA, KSA, and MA Test Modem (TM) requirements to the IEC performance specification for the TM. Requirements are traced by service, SSA, KSA, and MA.

	SSA REQUIREMENTS	
GE, SSA HWCI Paragraph	Title	IEC Unit Paragraph
3.0	REQUIREMENTS	Title
3.1	Hardware Configuration Item Definition	Description
3.1.1	Item Functions	Introduction
3.1.1.1	Integrated Receiver (IR)	N/A
3.1.1.2	Modulator/Doppler Predictor (MDP)	N/A
3.1.1.3	PTE	Introduction
3.1.2	Major Equipment List	N/A
3.1.3	Interface Definition and Characteristics	Title
3.1.3.1	Integrated Receiver	N/A
3.1.3.2	Modulator/Doppler Predictor (MDP)	N/A
3.1.3.3	PTE	Title
3.1.3.3.1	Interfaces	Title
3.1.3.3.1.1	AC Power	3.1.2.2.1
3.1.3.3.1.2	1553B Data Bus	3.1.2.2.2
3.1.3.3.1.3	Common Time and Frequency Inputs	3.1.2.2.3
3.1.3.3.1.4	PTE 370 MHz IF Output	3.1.2.2.4
3.1.3.3.1.5	PTE Modulated 8.5 MHz IF Output	3.1.2.2.5
3.1.3.3.1.6	PTE I and Q Recovery Return Data/Clock Inputs	3.1.2.2.6
3.1.3.3.1.7	PTE Simulated Command Data/Clock Outputs	3.1.2.2.7
3.1.3.3.1.8	PTE Low Data Rate Baseband Data Outputs	3.1.2.2.8
3.1.3.3.1.9	PTE I and Q Simulated User Return Data and Clock Input	3.1.2.2.9
3.1.3.3.1.10	PTE Recovered Forward Data and Clock Output	3.1.2.2.10
3.1.3.3.1.11	PTE 370 MHz IF Input	3.1.2.2.11
3.1.3.3.1.12	Data Transmission Test Sets (BERTs) Interfaces to the Test Modem	Title
3.1.3.3.1.12.1	XMIT Clock Output	3.1.2.3.1
3.1.3.3.1.12.2	Data Inputs	3.1.2.3.2
3.1.3.3.1.12.3	Recovered Data and Clock Outputs	3.1.2.3.3
3.1.3.3.1.13	Noise and Interference Test Set Interfaces to the Test Modem	Title
3.1.3.3.1.13.1	Test Modem IF Output	3.1.2.3.4
3.1.3.3.1.13.2	Test Modem IF Input	3.1.2.3.5
3.1.3.3.1.14	IEEE-488 Interfaces to the Test Modem	3.1.2.3.6
3.1.4	Government Furnished Equipment	3.1.4
3.1.5	Customer Furnished Equipment	N/A
3.2	Characteristics	Title
3.2.1	Performance Characteristics	Introduction
3.2.1.1	Integrated Receiver	N/A

GE, SSA HWCI Paragraph	SSA Requirements (Continued) Title	IEC Unit Paragraph
3.2.1.3	PMM Test Equipment	Introduction
3.2.1.3.1	PTE Forward Demodulator	Title
3.2.1.3.1.1	Application	Description
3.2.1.3.1.2	Input Signal Description	3.2.1.1.1.1
3.2.1.3.1.2.1	Input Data Configurations	3.2.1.1.1.1
3.2.1.3.1.2.2	Input Signal Distortions	3.2.1.1.1.2
3.2.1.3.1.2.3	C/N_o Dynamic Range	3.2.1.1.1.2.2, 3,4
3.2.1.3.1.3	Operations	Title
3.2.1.3.1.3.1	Commanding	3.2.1.1.1
3.2.1.3.1.3.1.1	Configuration Commands	Description
3.2.1.3.1.3.1.2	Frequency and Delay Profiles	3.2.1.1.1.3
3.2.1.3.1.3.1.3	PTE Demod Control Commands	3.1.2.2.2.a(2)
3.2.1.3.1.3.2	Operating States	3.1.2.2.2.2
3.2.1.3.1.4	Functions	3.1
3.2.1.3.1.5	Performance Requirements	Introduction
3.2.1.3.1.5.1	Test Data and Clock Generation	3.2.1.1.6
3.2.1.3.1.5.2	Acquisition	3.2.1.1.2.1
3.2.1.3.1.5.3	SSAF Range Channel Reacquisition	3.2.1.1.2.4
3.2.1.3.1.5.4	Cycle Slippage	3.2.1.1.4.1.1
3.2.1.3.1.5.5	Symbol/Decoder Synchronization	3.2.1.1.3.3
3.2.1.3.1.5.6	Bit Slippage	3.2.1.1.4.1.2
3.2.1.3.1.5.7	Probability of Error	Title
3.2.1.3.1.5.7.1	Definition	Title
3.2.1.3.1.5.7.1.1	Minimum Required Channel C/N_o	3.2.1.1.1.2.3
3.2.1.3.1.5.7.2	Requirements	Title
3.2.1.3.1.5.7.2.1	Bit Error Probability	3.2.1.1.1.2.3
3.2.1.3.1.5.7.2.2	Applicability	3.2.1.1.1.2.3
3.2.1.3.1.5.8	E_b/N_o Estimate	3.2.1.1.4.3
3.2.1.3.1.5.9	BER Measurement	3.2.1.1.6.1
3.2.1.3.1.5.10	Frequency and Delay Profiles	3.2.1.2.6.1a
3.2.1.3.1.5.11	Forward Model	3.1.2.2.2.3
3.2.1.3.1.6	Tracking Services	Introduction
3.2.1.3.1.6.1	Range Delay Measurement	3.2.1.1.5.1
3.2.1.3.1.6.1.1	Description	3.2.1.1.5.1.1
3.2.1.3.1.6.1.2	Services	3.2.1.1.5.1
3.2.1.3.1.6.1.3	Random Error	3.2.1.1.5.1.2
3.2.1.3.1.6.1.4	Systematic Error	3.2.1.1.5.1.3
3.2.1.3.1.6.1.5	Reporting	3.2.1.1.5.1.4
3.2.1.3.1.6.2	Doppler Measurement	3.2.1.1.5.2
3.2.1.3.1.6.2.1	Description	3.2.1.1.5.2.1
3.2.1.3.1.6.2.2	Services	3.2.1.1.5.1
3.2.1.3.1.6.2.3	Measurement Error	3.2.1.1.5.2.2
3.2.1.3.1.6.2.4	(Not Used)	N/A
3.2.1.3.1.6.2.5	(Not Used)	N/A
3.2.1.3.1.6.2.6	Reporting	3.2.1.1.5.2.3

GE, SSA HWCI Paragraph	SSA Requirements (Continued) Title	IEC Unit Paragraph
3.2.1.3.1.7	Performance Measuring and Monitoring Support	3.1.2.4.1,2,3; 3.2.1.3.2.3, 3.1.2.2.2
3.2.1.3.2	PTE Return Modulator	Title
3.2.1.3.2.1	Application	3.1.1.2
3.2.1.3.2.2	Input Signal Description	3.1.2.1.3
3.2.1.3.2.3	Operations	Title
3.2.1.3.2.3.1	Commanding	3.2.1.1.1
3.2.1.3.2.3.1.1	Configuration Commands	Description
3.2.1.3.2.3.1.2	Frequency Profile	3.2.1.2.6.1
3.2.1.3.2.3.1.3	Control Commands	3.1.2.2.2
3.2.1.3.2.3.2	Operating States	3.1.2.2.2.2
3.2.1.3.2.4	Functions	3.1
3.2.1.3.2.5	Performance Requirements	Introduction
3.2.1.3.2.5.1	Internal Test Data and Clock Generation	3.2.1.1.6
3.2.1.3.2.5.2	Input Data and Clock Synchronization	3.2.1.2.c
3.2.1.3.2.5.3	Data Processing Configurations and Modulation Formats	3.2.1.2.1
3.2.1.3.2.5.4	PN Codes	3.2.1.2.4
3.2.1.3.2.5.5	Error Correction Coding	3.2.1.2.3.2
3.2.1.3.2.5.6	Interleaving	3.2.1.2.3.4
3.2.1.3.2.5.7	PN Spreading and Modulation	3.2.1.2.4.2
3.2.1.3.2.5.7.1	Independently Generated Carrier	3.2.1.2.6.1
3.2.1.3.2.5.7.2	Coherently Derived Carrier	3.2.1.2.6.1
3.2.1.3.2.5.8	Carrier I/Q Phase Relationship	3.2.1.2.5.1a
3.2.1.3.2.5.9	I:Q Power Ratio	3.2.1.2.5.1b
3.2.1.3.2.5.10	Carrier-to-Noise Ratio	3.2.1.2.5.2
3.2.1.3.2.5.11	BER Measurement	3.2.1.2.7
3.2.1.3.2.5.12	Data Delay Measurement	3.2.1.2.8
3.2.1.3.2.6	(Not Used)	N/A
3.2.1.3.2.7	Performance Measuring and Monitoring Support	3.2.1.3
3.2.2	Physical Characteristics	3.2.2
3.2.2.1	Size	3.2.2.1
3.2.2.2	Weight	3.2.2.2
3.2.2.3	Packaging	3.2.2
3.2.2.3.1	Rack Packaging	N/A
3.2.2.3.2	Chassis Packaging	3.2.2,3.2.2.1, 3.3.1.5
3.2.2.4	Cabling	3.2.2
3.2.2.5	Cooling	N/A
3.2.2.6	Acoustical Noise	3.2.3.3
3.2.3	Reliability	3.2.3
3.2.3.1	Mean Time Between Failures (MTBF)	3.2.3,3.2.3.1
3.2.3.2	Design Life	3.2.3.2
3.2.3.3	Operational Capability	N/A

GE, SSA HWCI Paragraph	SSA Requirements (Continued) Title	IEC Unit Paragraph
3.2.4	Maintainability	3.2.4
3.2.4.1	Line Replaceable Unit (LRU) Replacement	3.2.4.1
3.2.4.1.1	LRU Definition	3.2.4.1.1
3.2.4.2	Mean Time To Repair (MTTR)	3.2.4.2
3.2.4.3	Maximum Time To Repair (MTR)	3.2.4.3
3.2.4.4	Self-Test	3.2.1.8.1
3.2.4.4.1	Confidence Test	3.2.1.8.2.1
3.2.4.4.2	Operational Status	3.2.1.8
3.2.4.4.3	Isolation of a Malfunction	3.5.1.3,3.5.1.2, & 3.5.1.3.1
3.2.4.4.4	Fault Isolation Performance Requirements	N/A
3.2.4.4.5	Test via Standard Commercial Test Equipment	3.5.1.3
3.2.4.4.6	Fault Isolation Using Extended BIT	3.2.1.3.2.2
3.2.4.5	Maintainability Demonstration	N/A
3.2.5	Environmental Conditions	Title
3.2.5.1	Non-Operating – Shipping and Storage	3.2.5.1
3.2.5.1.1	Temperature	3.2.5.1a
3.2.5.1.2	Humidity	3.2.5.1b
3.2.5.1.3	Altitude	3.2.5.1c
3.2.5.1.4	Solar Radiation	3.2.5.1d
3.2.5.2	Operating – Environmentally Controlled Area	3.2.5.2
3.2.5.2.1	Temperature	3.2.5.2a
3.2.5.2.2	Humidity	3.2.5.2b
3.2.5.2.3	Altitude	3.2.5.2c
3.2.6	Transportability	3.2.6
3.3	Design and Construction	3.3
3.3.1	Parts, Materials and Processes	3.3.1
3.3.1.1	Standard and Non-Standard Parts and Materials	3.3.1.2
3.3.1.1.1	Standard Parts and Materials	3.3.1.2.1
3.3.1.1.2	Non-Standard Parts and Materials	3.3.1.2.2
3.3.1.1.3	Programming and Handling of Semiconductor Devices	3.3.1.2.4
3.3.1.2	Standard Components	3.3.1.2.3
3.3.2	Electrical Design	Title
3.3.2.1	Electrical Connections	Title
3.3.2.1.1	Attachment of Wires and Leads	3.3.1.7.1.1
3.2.2.1.2	Solderless Wrap	3.3.1.7.1.2
3.3.2.1.3	Soldered Connections	3.3.1.7.1.3
3.3.2.2	Electrical/Electronic Parts	3.3.1.7.2
3.3.2.3	Electrical Power	3.3.1.7.3
3.3.2.3.1	Single-Phase Power	3.3.6.1,3.1.2.1, 3.3.1.7.3.1
3.3.2.3.2	Power Cable Connections	N/A
3.3.2.3.3	Power Transient Susceptibility	3.3.1.7.3.2
3.3.2.3.4	Rack Mounted Chassis Power	N/A

GE, SSA HWCI Paragraph	SSA Requirements (Continued) Title	IEC Unit Paragraph
3.3.2.3.5	Overload Protection	3.3.1.7.3.3
3.3.2.3.5.1	Primary Circuit Fuses	3.3.1.7.3.4
3.3.2.3.5.2	Circuit Breakers	3.3.1.7.3.5
3.3.2.3.6	Power Loss Reporting	N/A
3.3.2.3.7	Batteries	N/A
3.3.2.4	Printed Wiring	3.3.1.7.4
3.3.2.4.1	Single or Double-Sided Printed Wiring Boards	3.3.1.7.5
3.3.2.4.2	Multilayer Printed Wiring Boards	3.3.1.7.6
3.3.2.5	Preferred Circuits	3.3.1.7.7
3.3.2.6	Arc Suppression	N/A
3.3.3	Mechanical Design	Title
3.3.3.1	Accessibility	3.3.1.8.1
3.3.3.2	Structural Integrity	3.3.1.8.2
3.3.3.3	Captive Hardware	3.3.1.8.3
3.3.3.4	Coating, Treatment and Painting	3.3.1.4 & 3.3.1.3
3.3.3.5	Thermal Design	3.3.1.9
3.3.3.6	Structural Welding	N/A
3.3.4	Electromagnetic Compatibility (EMC) Control	3.3.2
3.3.4.1	EMI Development Testing	3.3.2.1
3.3.4.2	Commercial-Off-The-Shelf (COTS) Equipment EMC	N/A
3.3.5	Grounding, Bonding, and Shielding	3.3.1.5
3.3.6	Red/Black Isolation	N/A
3.3.7	Identification and Marking	3.3.3,3.3.1.6, 3.3.6
3.3.8	Workmanship	3.3.4
3.3.9	Interchangeability/Producibility	Title
3.3.9.1	Interchangeability	3.3.5.1
3.3.9.2	Producibility	3.3.5.2
3.3.10	Safety Criteria	3.3.6
3.3.10.1	Leakage Current	3.3.6.1
3.3.10.2	Power Supply Protection	3.3.6.2
3.3.10.3	Printed Circuit Assembly Protection	3.3.6.3.1
3.3.10.4	Equipment Electrical Power On-Off Switch	3.3.6.3
3.3.10.5	Power Indicator Lamp	3.3.6.4
3.3.10.6	Electrical Cable Protection	3.3.6.5
3.3.10.7	Support Strength	3.3.6.6
3.3.10.8	Equipment Access Security	3.3.6.7
3.3.10.9	Critical Controls	3.3.6.8
3.3.10.10	Human Error Design Protection	3.3.6.9
3.3.10.11	Unacceptable Materials	3.3.6.10
3.3.10.12	Test Circuit Protection	3.3.6.11
3.3.11	Human Engineering	3.3.7
3.3.12	Standards of Manufacture	N/A

GE, SSA HWCI Paragraph	SSA Requirements (Continued) Title	IEC Unit Paragraph
3.4	Documentation	N/A
3.5	Logistics	3.5
3.5.1	Maintenance Levels	N/A
3.5.1.1	On-Line Corrective Maintenance, First Level Maintenance	3.5.1.3
3.5.1.1.1	Use of the Maintenance Test Group (MTG)	N/A
3.5.1.1.2	In-Circuit Preventive Maintenance, First Level Maintenance	3.5.1.3.2
3.5.1.2	Off-Line Maintenance, Second Level Maintenance	N/A
3.5.1.2.1	Hardware Maintenance Depot (HMD)	N/A
3.5.1.2.2	Vendor Maintenance	N/A
3.5.1.2.2.1	On-Line Equipment Resupply	N/A
3.5.1.2.2.2	Configuration Management	N/A

GE, KSA HWCI Paragraph	KSA REQUIREMENTS Title	IEC Unit Paragraph
3.0	REQUIREMENTS	Title
3.1	Hardware Configuration Item Definition	Description
3.1.1	Item Functions	Introduction
3.1.1.1	Integrated Receiver (IR)	N/A
3.1.1.2	Modulator/Doppler Predictor (MDP)	N/A
3.1.1.3	PTE	Introduction
3.1.2	Major Equipment List	N/A
3.1.3	Interface Definition and Characteristics	Title
3.1.3.1	Integrated Receiver	N/A
3.1.3.2	Modulator/Doppler Predictor (MDP)	N/A
3.1.3.3	PTE	Title
3.1.3.3.1	External Interfaces	Title
3.1.3.3.1.1	AC Power	3.1.2.2.1
3.1.3.3.1.2	1553B Data Bus	3.1.2.2.2
3.1.3.3.1.3	Common Time and Frequency Inputs	3.1.2.2.3
3.1.3.3.1.4	PTE 370 MHz IF Output	3.1.2.2.4
3.1.3.3.1.5	PTE 8.5 MHz IF Output	3.1.2.2.5
3.1.3.3.1.6	PTE Baseband Data/Clock Inputs	3.1.2.2.6
3.1.3.3.1.7	PTE Baseband Command Data/Clock Outputs	3.1.2.2.7
3.1.3.3.1.8	PTE Baseband Data Outputs	3.1.2.2.8
3.1.3.3.1.9	I and Q Simulated User Return Data and Clock Inputs	3.1.2.2.9
3.1.3.3.1.10	Recovered Forward Data and Clock Outputs	3.1.2.2.10
3.1.3.3.1.11	PTE 370 MHz IF Input	3.1.2.2.11
3.1.3.3.1.12	Data Transmission Test Sets (BERTs) Interfaces to the Test Modem	Title
3.1.3.3.1.12.1	XMIT Clock Output	3.1.2.3.1
3.1.3.3.1.12.2	Data Inputs	3.1.2.3.2
3.1.3.3.1.12.3	Recovered Data and Clock Outputs	3.1.2.3.3
3.1.3.3.1.13	Noise and Interference Test Set Interfaces to the Test Modem	Title
3.1.3.3.1.13.1	Test Modem IF Output	3.1.2.3.4
3.1.3.3.1.13.2	Test Modem IF Input	3.1.2.3.5
3.1.3.3.1.14	IEEE-488 Interfaces to the Test Modem	3.1.2.3.6
3.1.4	Government Furnished Equipment	3.1.4
3.1.5	Customer Furnished Equipment	N/A
3.2	Characteristics	Title
3.2.1	Performance Characteristics	Introduction
3.2.1.1	Integrated Receiver (UR)	N/A
3.2.1.2.2	MDP Performance Requirements	N/A
3.2.1.3	PMM Test Equipment	Introduction
3.2.1.3.1	PTE Forward Demodulator	Title
3.2.1.3.1.1	Application	Description
3.2.1.3.1.2	Input Signal Description	3.2.1.1.1.1
3.2.1.3.1.2.1	Input Data Configurations	3.2.1.1.1.1
3.2.1.3.1.2.2	Input Signal Distortions	3.2.1.1.1.2

GE, KSA HWCI Paragraph	KSA Requirements (Continued) Title	IEC Unit Paragraph
3.2.1.3.1.2.3	C/N_o Dynamic Range	3.2.1.1.1.2.2, 3,4
3.2.1.3.1.3	Operations	Title
3.2.1.3.1.3.1	Commanding	3.2.1.1.1
3.2.1.3.1.3.1.1	Configuration Commands	Description
3.2.1.3.1.3.1.2	Frequency and Delay Profiles	3.2.1.1.1.3
3.2.1.3.1.3.1.3	PTE Demod Control Commands	3.1.2.2.2.a(2)
3.2.1.3.1.3.2	Operating States	3.1.2.2.2.2
3.2.1.3.1.4	Functions	3.1
3.2.1.3.1.5	Performance Requirements	Introduction
3.2.1.3.1.5.1	Test Data and Clock Generation	3.2.1.1.6
3.2.1.3.1.5.2	Acquisition	3.2.1.1.2.1
3.2.1.3.1.5.3	KSAF Range Channel Reacquisition	3.2.1.1.2.4
3.2.1.3.1.5.4	Cycle Slippage	3.2.1.1.4.1.1
3.2.1.3.1.5.5	Symbol Synchronization	3.2.1.1.3.3
3.2.1.3.1.5.6	Bit Slippage	3.2.1.1.4.1.2
3.2.1.3.1.5.7	Probability of Error	Title
3.2.1.3.1.5.7.1	Definition	Title
3.2.1.3.1.5.7.1.1	Minimum Required Channel C/N_o	3.2.1.1.1.2.3
3.2.1.3.1.5.7.2	Requirements	Title
3.2.1.3.1.5.7.2.1	Bit Error Probability	3.2.1.1.1.2.3
3.2.1.3.1.5.7.2.2	Applicability	3.2.1.1.1.2.3
3.2.1.3.1.5.8	E_b/N_o Estimate	3.2.1.1.4.3
3.2.1.3.1.5.9	BER Measurement	3.2.1.1.6.1
3.2.1.3.1.5.10	Frequency and Delay Profiles	3.2.1.2.6.1a
3.2.1.3.1.5.11	Forward Model	3.1.2.2.2.3
3.2.1.3.1.6	Tracking Services	Introduction
3.2.1.3.1.6.1	Range Delay Measurement	3.2.1.1.5.1
3.2.1.3.1.6.1.1	Description	3.2.1.1.5.1.1
3.2.1.3.1.6.1.2	Services	3.2.1.1.5.1
3.2.1.3.1.6.1.3	Random Error	3.2.1.1.5.1.2
3.2.1.3.1.6.1.4	Systematic Error	3.2.1.1.5.1.3
3.2.1.3.1.6.1.5	Reporting	3.2.1.1.5.1.4
3.2.1.3.1.6.2	Doppler Measurement	3.2.1.1.5.2
3.2.1.3.1.6.2.1	Description	3.2.1.1.5.2.1
3.2.1.3.1.6.2.2	Services	3.2.1.1.5.1
3.2.1.3.1.6.2.3	Measurement Error	3.2.1.1.5.2.2
3.2.1.3.1.6.2.4	(Not Used)	N/A
3.2.1.3.1.6.2.5	(Not Used)	N/A
3.2.1.3.1.6.2.6	Reporting	3.2.1.1.5.2.3
3.2.1.3.1.7	Performance Measuring and Monitoring Support	3.1.2.4.1,2,3; 3.1.2.2.2
3.2.1.3.2	PTE Return Modulator	Title
3.2.1.3.2.1	Application	3.1.1.2
3.2.1.3.2.2	Input Signal Description	3.1.2.1.3
3.2.1.3.2.3	Operations	Title

GE, KSA HWCI Paragraph	KSA Requirements (Continued) Title	IEC Unit Paragraph
3.2.1.3.2.3.1	Commanding	3.2.1.1.1
3.2.1.3.2.3.1.1	Configuration Commands	Description
3.2.1.3.2.3.1.2	Frequency Profile	3.2.1.2.6.1
3.2.1.3.2.3.1.3	Control Commands	3.1.2.2.2
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3.2.1.3.2.4	Functions	3.1
3.2.1.3.2.5	Performance Requirements	Introduction
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3.2.1.3.2.5.4	PN Codes	3.2.1.2.4
3.2.1.3.2.5.5	Error Correction Coding	3.2.1.2.3.2
3.2.1.3.2.5.6	Interleaving	3.2.1.2.3.4
3.2.1.3.2.5.7	PN Spreading and Modulation	3.2.1.2.4.2
3.2.1.3.2.5.7.1	Independently Generated Carrier	3.2.1.2.6.1
3.2.1.3.2.5.7.2	Coherently Derived Carrier	3.2.1.2.6.1
3.2.1.3.2.5.8	Carrier I/Q Phase Relationship	3.2.1.2.5.1a
3.2.1.3.2.5.9	I:Q Power Ratio	3.2.1.2 5.1b
3.2.1.3.2.5.10	Carrier-to-Noise Ratio	3.2.1.2.5.2
3.2.1.3.2.5.11	BER Measurement	3.2.1.2.7
3.2.1.3.2.5.12	Data Delay Measurement	3.2.1.2.8
3.2.1.3.2.6	(Not Used)	N/A
3.2.1.3.2.7	Performance Measuring and Monitoring Support	3.2.1.3
3.2.2	Physical Characteristics	3.2.2
3.2.2.1	Size	3.2.2.1
3.2.2.2	Weight	3.2.2.2
3.2.2.3	Packaging	3.2.2
3.2.2.3.1	Rack Packaging	N/A
3.2.2.3.2	Chassis Packaging	3.2.2,3.2.2.1 3.3.3, 3.3.1.5
3.2.2.4	Cabling	3.2.2
3.2.2.5	Cooling	N/A
3.2.2.6	Acoustical Noise	3.2.3.3
3.2.3	Reliability	3.2.3
3.2.3.1	Mean Time Between Failures (MTBF)	3.2.3,3.2.3.1
3.2.3.2	Design Life	3.2.3.2
3.2.3.3	Operational Capability	N/A
3.2.4	Maintainability	3.2.4
3.2.4.1	Line Replaceable Unit (LRU) Replacement	3.2.4.1
3.2.4.1.1	LRU Definition	3.2.4.1.1
3.2.4.2	Mean Time To Repair (MTTR)	3.2.4.2
3.2.4.3	Maximum Time To Repair (MTR)	3.2.4.3
3.2.4.4	Self-Test	3.2.1.8.1
3.2.4.4.1	Confidence Test	3.2.1.8.2.1
3.2.4.4.2	Operational Status	3.2.1.8

GE, KSA HWCI Paragraph	KSA Requirements (Continued) Title	IEC Unit Paragraph
3.2.4.4.3	Isolation of a Malfunction	3.5.1.3,3.5.1.2, & 3.5.1.3.1
3.2.4.4.4	Fault Isolation Performance Requirements	N/A
3.2.4.4.5	Test via Standard Commercial Test Equipment	3.5.1.3
3.2.4.4.6	Fault Isolation Using Extended BIT	3.2.1.3.2.2
3.2.4.5	Maintainability Demonstration	N/A
3.2.5	Environmental Conditions	Title
3.2.5.1	Non-Operating – Shipping and Storage	3.2.5.1
3.2.5.1.1	Temperature	3.2.5.1a
3.2.5.1.2	Humidity	3.2.5.1b
3.2.5.1.3	Altitude	3.2.5.1c
3.2.5.1.4	Solar Radiation	3.2.5.1d
3.2.5.2	Operating – Environmentally Controlled Area	3.2.5.2
3.2.5.2.1	Temperature	3.2.5.2a
3.2.5.2.2	Humidity	3.2.5.2b
3.2.5.2.3	Altitude	3.2.5.2c
3.2.6	Transportability	3.2.6
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3.3.1	Parts, Materials and Processes	3.3.1
3.3.1.1	Standard and Non-Standard Parts and Materials	3.3.1.2
3.3.1.1.1	Standard Parts and Materials	3.3.1.2.1
3.3.1.1.2	Non-Standard Parts and Materials	3.3.1.2.2
3.3.1.1.3	Programming and Handling of Semiconductor Devices	3.3.1.2.4
3.3.1.2	Standard Components	3.3.1.2.3
3.3.2	Electrical Design	Title
3.3.2.1	Electrical Connections	Title
3.3.2.1.1	Attachment of Wires and Leads	3.3.1.7.1.1
3.2.2.1.2	Solderless Wrap	3.3.1.7.1.2
3.3.2.1.3	Soldered Connections	3.3.1.7.1.3
3.3.2.2	Electrical/Electronic Parts	3.3.1.7.2
3.3.2.3	Electrical Power	3.3.1.7.3
3.3.2.3.1	Single-Phase Power	3.3.6.1,3.1.2.1, 3.3.1.7.3.1
3.3.2.3.2	Power Cable Connections	N/A
3.3.2.3.3	Power Transient Susceptibility	3.3.1.7.3.2
3.3.2.3.4	Rack Mounted Chassis Power	N/A
3.3.2.3.5	Overload Protection	3.3.1.7.3.3
3.3.2.3.5.1	Primary Circuit Fuses	3.3.1.7.3.4
3.3.2.3.5.2	Circuit Breakers	3.3.1.7.3.5
3.3.2.3.6	Power Loss Reporting	N/A
3.3.2.3.7	Batteries	N/A
3.3.2.4	Printed Wiring	3.3.1.7.4
3.3.2.4.1	Single or Double-Sided Printed Wiring Boards	3.3.1.7.5
3.3.2.4.2	Multilayer Printed Wiring Boards	3.3.1.7.6

GE, KSA HWCI Paragraph	KSA Requirements (Continued) Title	IEC Unit Paragraph
3.3.2.5	Preferred Circuits	3.3.1.7.7
3.3.2.6	Arc Suppression	N/A
3.3.3	Mechanical Design	Title
3.3.3.1	Accessibility	3.3.1.8.1
3.3.3.2	Structural Integrity	3.3.1.8.2
3.3.3.3	Captive Hardware	3.3.1.8.3
3.3.3.4	Coating, Treatment and Painting	3.3.1.4 & 3.3.1.3
3.3.3.5	Thermal Design	3.3.1.9
3.3.3.6	Structural Welding	N/A
3.3.4	Electromagnetic Compatibility (EMC) Control	3.3.1.3, 3.3.2
3.3.4.1	EMI Development Testing	3.3.2.1
3.3.4.2	Commercial-Off-The-Shelf (COTS) Equipment EMC	N/A
3.3.5	Grounding, Bonding, and Shielding	3.3.1.5
3.3.6	Red/Black Isolation	N/A
3.3.7	Identification and Marking	3.3.3,3.3.1.6, 3.3.6
3.3.8	Workmanship	3.3.4
3.3.9	Interchangeability/Producibility	Title
3.3.9.1	Interchangeability	3.3.5.1
3.3.9.2	Producibility	3.3.5.2
3.3.10	Safety Criteria	3.3.6
3.3.10.1	Leakage Current	3.3.6.1
3.3.10.2	Power Supply Protection	3.3.6.2
3.3.10.3	Printed Circuit Assembly Protection	3.3.6.3.1
3.3.10.4	Equipment Electrical Power On-Off Switch	3.3.6.3
3.3.10.5	Power Indicator Lamp	3.3.6.4
3.3.10.6	Electrical Cable Protection	3.3.6.5
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3.3.10.8	Equipment Access Security	3.3.6.7
3.3.10.9	Critical Controls	3.3.6.8
3.3.10.10	Human Error Design Protection	3.3.6.9
3.3.10.11	Unacceptable Materials	3.3.6.10
3.3.10.12	Test Circuit Protection	3.3.6.11
3.3.11	Human Engineering	3.3.7
3.3.12	Standards of Manufacture	N/A
3.4	Documentation	N/A
3.5	Logistics	3.5
3.5.1	Maintenance Levels	N/A
3.5.1.1	On-Line Corrective Maintenance, First Level Maintenance	3.5.1.3
3.5.1.1.1	Use of the Maintenance Test Group (MTG)	N/A
3.5.1.1.2	In-Circuit Preventive Maintenance, First Level Maintenance	3.5.1.3.2
3.5.1.2	Off-Line Maintenance, Second Level Maintenance	N/A
3.5.1.2.1	Hardware Maintenance Depot (HMD)	N/A

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3.5.1.2.2	Vendor Maintenance	N/A
3.5.1.2.2.1	On-Line Equipment Resupply	N/A
3.5.1.2.2.2	Configuration Management	N/A

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3.0	REQUIREMENTS	Title
3.1	Hardware Configuration Item Definition	Description
3.1.1	Item Functions	Introduction
3.1.1.1	Integrated Receiver (IR)	N/A
3.1.1.2	Modulator/Doppler Predictor (MDP)	N/A
3.1.1.3	PTE	Introduction
3.1.2	Major Equipment List	N/A
3.1.3	Interface Definition and Characteristics	Title
3.1.3.1	Integrated Receiver	N/A
3.1.3.2	Modulator/Doppler Predictor (MDP)	N/A
3.1.3.3	PTE	Title
3.1.3.3.1	External Interfaces	Title
3.1.3.3.1.2	1553B Data Bus	3.1.2.2.2
3.1.3.3.1.3	Common Time and Frequency Inputs	3.1.2.2.3
3.1.3.3.1.4	370 MHz IF Output	3.1.2.2.4
3.1.3.3.1.5	8.5 MHz IF Output	3.1.2.2.5
3.1.3.3.1.6	PTE Baseband Data/Clock Inputs	3.1.2.2.6
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3.1.3.3.1.9	I and Q Simulated User Return Data and Clock Inputs	3.1.2.2.9
3.1.3.3.1.10	Recovered Forward Data and Clock Outputs	3.1.2.2.10
3.1.3.3.1.11	Modulator 370 MHz IF Input	3.1.2.2.11
3.1.3.3.1.12	Data Transmission Test Sets (BERTs) Interfaces to the Test Modem	Title
3.1.3.3.1.12.1	XMIT Clock Output	3.1.2.3.1
3.1.3.3.1.12.2	Data Inputs	3.1.2.3.2
3.1.3.3.1.12.3	Recovered Data and Clock Outputs	3.1.2.3.3
3.1.3.3.1.13	Noise and Interference Test Set Interfaces to the Test Modem	Title
3.1.3.3.1.13.1	Test Modem IF Output	3.1.2.3.4
3.1.3.3.1.13.2	Test Modem IF Input	3.1.2.3.5
3.1.3.3.1.14	IEEE-488 Interfaces to the Test Modem	3.1.2.3.6
3.1.4	Government Furnished Equipment	3.1.4
3.1.5	Customer Furnished Equipment	N/A
3.2	Characteristics	Title
3.2.1	Performance Characteristics	Introduction
3.2.1.3	PMM Test Equipment	Introduction
3.2.1.3.1	PTE Forward Demodulator	Title
3.2.1.3.1.1	Application	Description
3.2.1.3.1.2	Input Signal Description	3.2.1.1.1.1
3.2.1.2.1.2.1	Input Data Configurations	3.2.1.1.1.1
3.2.1.3.1.2.2	Input Signal Distortions	3.2.1.1.1.2
3.2.1.3.1.2.3	C/N_o Dynamic Range	3.2.1.1.1.2.2, 3,4
3.2.1.3.1.3	Operations	Title

GE, MA HWCI Paragraph	MA Requirements (Continued) Title	IEC Unit Paragraph
3.2.1.3.1.3.1	Commanding	3.2.1.1.1
3.2.1.3.1.3.1.1	Configuration Commands	Description
3.2.1.3.1.3.1.2	Frequency and Delay Profiles	3.2.1.1.1.3
3.2.1.3.1.3.1.3	PTE Demod Control Commands	3.1.2.2.2.a(2)
3.2.1.3.1.3.1.4	Operating States	3.1.2.2.2.2
3.2.1.3.1.4	Functions	3.1
3.2.1.3.1.5	Performance Requirements	Introduction
3.2.1.3.1.5.1	Test Data and Clock Generation	3.2.1.1.6
3.2.1.3.1.5.2	Acquisition	3.2.1.1.2.1
3.2.1.3.1.5.3	MAF Range Channel Reacquisition	3.2.1.1.2.4
3.2.1.3.1.5.4	Cycle Slippage	3.2.1.1.4.1.1
3.2.1.3.1.5.5	Symbol Synchronization (Uncoded Data Only)	3.2.1.1.3.3
3.2.1.3.1.5.6	Bit Slippage	3.2.1.1.4.1.2
3.2.1.3.1.5.7	Probability of Error	Title
3.2.1.3.1.5.7.1	Definition	Title
3.2.1.3.1.5.7.1.1	Minimum Required Channel C/N_o	3.2.1.1.1.2.3
3.2.1.3.1.5.7.2	Requirements	Title
3.2.1.3.1.5.7.2.1	Bit Error Probability	3.2.1.1.1.2.3
3.2.1.3.1.5.7.2.2	Applicability	3.2.1.1.1.2.3
3.2.1.3.1.5.8	E_b/N_o Estimate	3.2.1.1.4.3
3.2.1.3.1.5.9	BER Measurement	3.2.1.1.6.1
3.2.1.3.1.5.10	Frequency and Delay Profiles	3.2.1.2.6.1a
3.2.1.3.1.5.11	Forward Model	3.1.2.2.2.3
3.2.1.3.1.6	Tracking Services	Introduction
3.2.1.3.1.6.1	Range Delay Measurement	3.2.1.1.5.1
3.2.1.3.1.6.1.1	Description	3.2.1.1.5.1.1
3.2.1.3.1.6.1.2	Services	3.2.1.1.5.1
3.2.1.3.1.6.1.3	Random Error	3.2.1.1.5.1.2
3.2.1.3.1.6.1.4	Systematic Error	3.2.1.1.5.1.3
3.2.1.3.1.6.1.5	Reporting	3.2.1.1.5.1.4
3.2.1.3.1.6.2	Doppler Measurement	3.2.1.1.5.2
3.2.1.3.1.6.2.1	Description	3.2.1.1.5.2.1
3.2.1.3.1.6.2.2	Services	3.2.1.1.5.1
3.2.1.3.1.6.2.3	Measurement Error	3.2.1.1.5.2.2
3.2.1.3.1.6.2.4	(Not Used)	N/A
3.2.1.3.1.6.2.5	(Not Used)	N/A
3.2.1.3.1.6.2.6	Reporting	3.2.1.1.5.2.3
3.2.1.3.1.7	Performance Measuring and Monitoring Support	3.1.2.4.1,2,3; 3.1.2.2.2
3.2.1.3.2	PTE Return Modulator	Title
3.2.1.3.2.1	Application	3.1.1.2
3.2.1.3.2.2	Input Signal Description	3.1.2.1.3
3.2.1.3.2.3	Operations	Title
3.2.1.3.2.3.1	Commanding	3.2.1.1.1
3.2.1.3.2.3.1.1	Configuration Commands	Description
3.2.1.3.2.3.1.2	Frequency Profile	3.2.1.2.6.1

GE, MA HWCI Paragraph	MA Requirements (Continued) Title	IEC Unit Paragraph
3.2.1.3.2.3.1.3	Control Commands	3.1.2.2.2
3.2.1.3.2.3.2	Operating States	3.1.2.2.2.2
3.2.1.3.2.4	Functions	3.1
3.2.1.3.2.5	Performance Requirements	Introduction
3.2.1.3.2.5.1	Internal Test Data and Clock Generation	3.2.1.1.6
3.2.1.3.2.5.2	Input Data and Clock Synchronization	3.2.1.2.c
3.2.1.3.2.5.3	Data Processing Configurations and Modulation Formats	3.2.1.2.1
3.2.1.3.2.5.4	PN Codes	3.2.1.2.4
3.2.1.3.2.5.5	Error Correction Coding	3.2.1.2.3.2
3.2.1.3.2.5.6	Interleaving	3.2.1.2.3.4
3.2.1.3.2.5.7	PN Spreading and Modulation	3.2.1.2.4.2
3.2.1.3.2.5.7.1	Independently Generated Carrier	3.2.1.2.6.1
3.2.1.3.2.5.7.2	Coherently Derived Carrier	3.2.1.2.6.1
3.2.1.3.2.5.8	Carrier I/Q Phase Relationship	3.2.1.2.5.1a
3.2.1.3.2.5.9	I:Q Power Ratio	3.2.1.2.5.1b
3.2.1.3.2.5.10	Carrier-to-Noise Ratio	3.2.1.2.5.2
3.2.1.3.2.5.11	BER Measurement	3.2.1.2.7
3.2.1.3.2.5.12	Data Delay Measurement	3.2.1.2.8
3.2.1.3.2.6	(Not Used)	N/A
3.2.1.3.2.7	Performance Measuring and Monitoring Support	3.2.1.3
3.2.2	Physical Characteristics	3.2.2
3.2.2.1	Size	3.2.2.1
3.2.2.2	Weight	3.2.2.2
3.2.2.3	Packaging	3.2.2
3.2.2.3.1	Rack Packaging	N/A
3.2.2.3.2	Chassis Packaging	3.2.2,3.2.2.1 3.3.1.5
3.2.2.4	Cabling	3.2.2
3.2.2.5	Cooling	N/A
3.2.2.6	Acoustical Noise	3.2.3.3
3.2.3	Reliability	3.2.3
3.2.3.1	Mean Time Between Failures (MTBF)	3.2.3,3.2.3.1
3.2.3.2	Design Life	3.2.3.2
3.2.3.3	Operational Capability	N/A
3.2.4	Maintainability	3.2.4
3.2.4.1	Line Replaceable Unit (LRU) Replacement	3.2.4.1
3.2.4.1.1	LRU Definition	3.2.4.1.1
3.2.4.2	Mean Time To Repair (MTTR)	3.2.4.2
3.2.4.3	Maximum Time To Repair (MTR)	3.2.4.3
3.2.4.4	Self-Test	3.2.1.8.1
3.2.4.4.1	Confidence Test	3.2.1.8.2.1
3.2.4.4.2	Operational Status	3.2.1.8
3.2.4.4.3	Isolation of a Malfunction	3.5.1.3,3.5.1.2, & 3.5.1.3.1
3.2.4.4.4	Fault Isolation Performance Requirements	N/A

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3.2.4.4.5	Test via Standard Commercial Test Equipment	3.5.1.3
3.2.4.4.6	Fault Isolation Using Extended BIT	3.2.1.3.2.2
3.2.4.5	Maintainability Demonstration	N/A
3.2.5	Environmental Conditions	Title
3.2.5.1	Non-Operating – Shipping and Storage	3.2.5.1
3.2.5.1.1	Temperature	3.2.5.1a
3.2.5.1.2	Humidity	3.2.5.1b
3.2.5.1.3	Altitude	3.2.5.1c
3.2.5.1.4	Solar Radiation	3.2.5.1d
3.2.5.2	Operating – Environmentally Controlled Area	3.2.5.2
3.2.5.2.1	Temperature	3.2.5.2a
3.2.5.2.2	Humidity	3.2.5.2b
3.2.5.2.3	Altitude	3.2.5.2c
3.2.6	Transportability	3.2.6
3.3	Design and Construction	3.3
3.3.1	Parts, Materials and Processes	3.3.1
3.3.1.1	Standard and Non-Standard Parts and Materials	3.3.1.2
3.3.1.1.1	Standard Parts and Materials	3.3.1.2.1
3.3.1.1.2	Non-Standard Parts and Materials	3.3.1.2.2
3.3.1.1.3	Programming and Handling of Semiconductor Devices	3.3.1.2.4
3.3.1.2	Standard Components	3.3.1.2.3
3.3.2	Electrical Design	Title
3.3.2.1	Electrical Connections	Title
3.3.2.1.1	Attachment of Wires and Leads	3.3.1.7.1.1
3.2.2.1.2	Solderless Wrap	3.3.1.7.1.2
3.3.2.1.3	Soldered Connections	3.3.1.7.1.3
3.3.2.2	Electrical/Electronic Parts	3.3.1.7.2
3.3.2.3	Electrical Power	3.3.1.7.3
3.3.2.3.1	Single-Phase Power	3.3.6.1,3.1.2.1, 3.3.1.7.3.1
3.3.2.3.2	Power Cable Connections	N/A
3.3.2.3.3	Power Transient Susceptibility	3.3.1.7.3.2
3.3.2.3.4	Rack Mounted Chassis Power	N/A
3.3.2.3.5	Overload Protection	3.3.1.7.3.3
3.3.2.3.5.1	Primary Circuit Fuses	3.3.1.7.3.4
3.3.2.3.5.2	Circuit Breakers	3.3.1.7.3.5
3.3.2.3.6	Power Loss Reporting	N/A
3.3.2.3.7	Batteries	N/A
3.3.2.4	Printed Wiring	3.3.1.7.4
3.3.2.4.1	Single or Double-Sided Printed Wiring Boards	3.3.1.7.5
3.3.2.4.2	Multilayer Printed Wiring Boards	3.3.1.7.6
3.3.2.5	Preferred Circuits	3.3.1.7.7
3.3.2.6	Arc Suppression	N/A
3.3.3	Mechanical Design	Title

GE, MA HWCI Paragraph	MA Requirements (Continued) Title	IEC Unit Paragraph
3.3.3.1	Accessibility	3.3.1.8.1
3.3.3.2	Structural Integrity	3.3.1.8.2
3.3.3.3	Captive Hardware	3.3.1.8.3
3.3.3.4	Coating, Treatment and Painting	3.3.1.4 & 3.3.1.3
3.3.3.5	Thermal Design	3.3.1.9
3.3.3.6	Structural Welding	N/A
3.3.4	Electromagnetic Compatibility (EMC) Control	3.3.2
3.3.4.1	EMI Development Testing	3.3.2.1
3.3.4.2	Commercial-Off-The-Shelf (COTS) Equipment EMC	N/A
3.3.5	Grounding, Bonding, and Shielding	3.3.1.5
3.3.6	Red/Black Isolation	N/A
3.3.7	Identification and Marking	3.3.3,3.3.1.6, 3.3.6
3.3.8	Workmanship	3.3.4
3.3.9	Interchangeability/Producibility	Title
3.3.9.1	Interchangeability	3.3.5.1
3.3.9.2	Producibility	3.3.5.2
3.3.10	Safety Criteria	3.3.6
3.3.10.1	Leakage Current	3.3.6.1
3.3.10.2	Power Supply Protection	3.3.6.2
3.3.10.3	Printed Circuit Assembly Protection	3.3.6.3.1
3.3.10.4	Equipment Electrical Power On-Off Switch	3.3.6.3
3.3.10.5	Power Indicator Lamp	3.3.6.4
3.3.10.6	Electrical Cable Protection	3.3.6.5
3.3.10.7	Support Strength	3.3.6.6
3.3.10.8	Equipment Access Security	3.3.6.7
3.3.10.9	Critical Controls	3.3.6.8
3.3.10.10	Human Error Design Protection	3.3.6.9
3.3.10.11	Unacceptable Materials	3.3.6.10
3.3.10.12	Test Circuit Protection	3.3.6.11
3.3.11	Human Engineering	3.3.7
3.3.12	Standards of Manufacture	N/A
3.4	Documentation	N/A
3.5	Logistics	3.5
3.5.1	Maintenance Levels	N/A
3.5.1.1	On-Line Corrective Maintenance, First Level Maintenance	3.5.1.3
3.5.1.1.1	Use of the Maintenance Test Group (MTG)	N/A
3.5.1.1.2	In-Circuit Preventive Maintenance, First Level Maintenance	3.5.1.3.2
3.5.1.2	Off-Line Maintenance, Second Level Maintenance	N/A
3.5.1.2.1	Hardware Maintenance Depot (HMD)	N/A
3.5.1.2.2	Vendor Maintenance	N/A
3.5.1.2.2.1	On-Line Equipment Resupply	N/A
3.5.1.2.2.2	Configuration Management	N/A

APPENDIX IV

40.0 TEST MATRIX

Reference STGT Unit Test Matrices, C901E3860.